

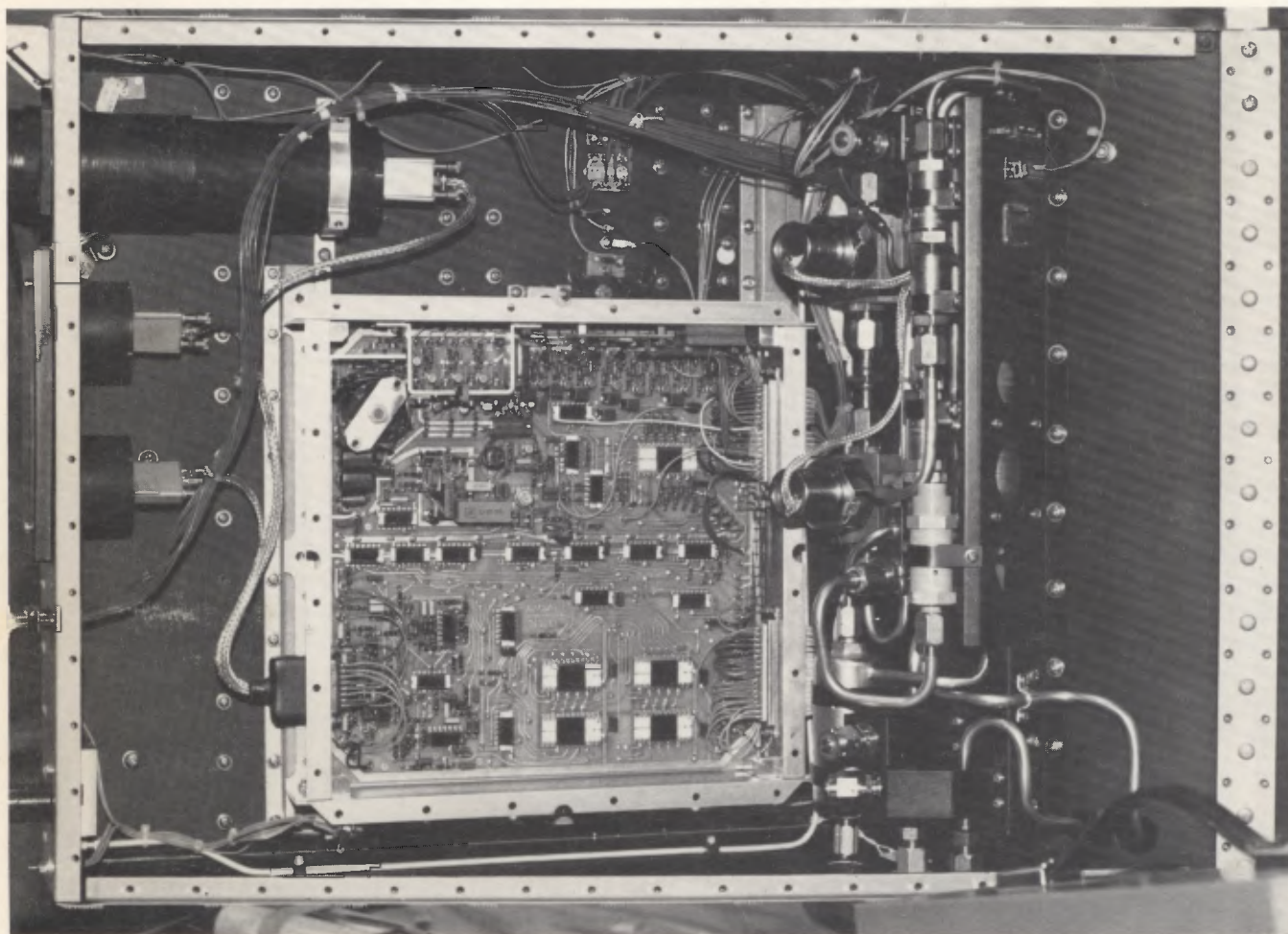
AMSAT-NA ***Technical Journal***

Volume 1, No. 1

Summer, 1987

A Look at the Phase-3C Spacecraft

Pages 13-14



AMSAT-NA Technical Journal

AMSAT-NA Technical Journal is a publication of the Radio Amateur Satellite Corporation of North America, AMSAT-NA. *AMSAT-NA Technical Journal* publishes papers reporting original work and significant findings in the fields of low-cost satellite design, construction, and operation, space communications, space sciences and related social value issues.

Contributions to *AMSAT-NA Technical Journal* are unrefereed working papers. Their content should be considered the personal opinion of the authors rather than organizational (company, any AMSAT group, etc.) unless otherwise noted. Readers who may wish to express their opinion on the content of an article may contact the author or the editor will forward their comments to the author.

Information for Authors and Editorial Address

Prospective authors are invited to submit articles for future issues of *AMSAT-NA Technical Journal*. Papers must contain a one paragraph abstract and be limited to ten pages (where possible) including graphs, tables and references. Preference will be given to unpublished works. Papers of general interest will be accepted for reprinting if the author includes documentation of the conditions of the original publisher for reprinting.

Material for publication should be submitted both in hardcopy form and as a text file on diskette. Any 5¼ inch format is acceptable provided the format is clearly indicated and all special character sequences used by word processors have been deleted from the text file. Figures should be drawn in a manner suitable for publication and larger than the size in which they will appear when published.

All material submitted to the Editor will be considered for publication unless otherwise requested. No material will be returned. A contribution to *AMSAT-NA Technical Journal* is welcomed from any person with an interest in the amateur radio space program. Contributions should be sent to:

Robert J. Diersing, N5AHD, Editor
AMSAT-NA Technical Journal
Corpus Christi State University
6300 Ocean Drive
Corpus Christi, TX 78412
(512)-991-6810 ext. 476

AMSAT-NA Technical Journal is published twice yearly in June and November for \$10 by AMSAT, 850 Sligo Ave., Suite 601, Silver Spring, MD 20910. POSTMASTER: Send address changes to *AMSAT-NA Technical Journal*, 850 Sligo Ave., Suite 601, Silver Spring, MD 20910.

Copyright © 1987 by AMSAT-NA, The Radio Amateur Satellite Corporation of North America. Contents may be reproduced without specific prior permission provided proper credit is given to the author and source and copies are sent to AMSAT-NA, the Editor, and the author. AMSAT is a registered trademark.

On the cover: Phase 3-C spacecraft.

Left side: Top large black tube, earth sensor.
Next two lower units, sun sensors.

These sensors provide input to the sensor electronics unit and the onboard computer in order to determine the attitude of the spacecraft in orbit.

Center: Sensor electronics unit module.

The SEU accepts input from the earth and sun sensors and processes it in conjunction with the onboard computer.

Right side: Propellant flow assembly.

The propellant flow assembly controls the flow of the fuel and oxidizer to the kick motor under control of the onboard computer and the liquid ignition unit.

The Radio Amateur Satellite Corporation of North America, AMSAT-NA Board of Directors

John Browning, W6SP, Chairman
Dr. Thomas A. Clark, W3IW1
John Henry, VE2VQ
Jan King, W3GEY
Harold Price, NK6K
Vern Riportella, WA2LQQ
Harry Yoneda, JA1ANG

AMSAT-NA Officers

Vern Riportella, WA2LQQ, President
John Champa, K8OCL, Executive Vice President
Jan King, W3GEY, Vice President, Engineering
Ralph Wallio, W0RPK, Vice President, Operations
Mike Crisler, N4IFD, Vice President, Field Operations
William Tynan, W3XO, Vice President,
Manned Space Operations
Art Feller, KB4ZJ, Treasurer
Martha Saragovitz, Secretary

Headquarters and Staff

AMSAT-NA
850 Sligo Ave., Suite 601
Silver Spring, MD 20910
Phone (301)-589-6062

Martha Saragovitz, Director of Administration

Table of Contents

<i>President's Message</i>	1
Vern Riportella, WA2LQQ	
<i>Editorial</i>	2
Robert J. Diersing, N5AHD	
<i>An Analysis of UoSAT-2 DCE Memory Performance</i>	4
Jeff W. Ward, G0/K8KA	
<i>A Look at the Phase-3C Spacecraft</i>	13
Robert J. Diersing, N5AHD and Jan King, W3GEY	
<i>BPSK Modulator for RUDAK Operation</i>	15
Knut Brenndoerfer, DF8CA	
<i>Satellite Telemetry Interface for 400 bit/s</i>	19
Karl Meinzer, DJ4ZC	
<i>Alignment of the AFREG Board</i>	23
Heinz Moelleken, DL3AH	
<i>A Proposed Series of Satellites for Digital Message Relay</i>	26
Gerry Creager, N5JXS	
<i>Power Budget and Eclipse Considerations for PTSE-H</i>	29
Courtney Duncan, N5BF	
<i>A Non-Cosmetic Improvement to the W3IWI Tracking Algorithm</i>	42
Robert W. McGwier, N4HY	

President's Message

AMSAT is privileged to have among its members some of the brightest minds in amateur radio and some of the best talent anywhere. Having brains and talent in an organization is one thing. Harnessing it and converting these assets to action and achievement is quite another matter. The key ingredient to harnessing brains and talent, I've learned, is instilling a communications discipline; a yearning to share ideas and concepts with others to promote growth and cross-pollenization.

A few years ago it became obvious to me we were collectively inadequate in communicating the ideas of the best and the brightest among us. This first edition of ATJ redresses that inadequacy in a significant first step.

When I asked Editor Bob Diersing to undertake this assignment, he promised to do his best. The result speaks for itself. Congratulations to Editor Diersing and the fine authors who have shared these excellent papers with us. My fondest hope and desire is that this edition should be but the first of a long series documenting the significant contributions made by the authors and their colleagues. Moreover, this record will illustrate the extent to which AMSAT has contributed to the advancement of amateur radio and ultimately to society at large whose spectrum we use in pursuit of our technical wizardry.

Vern Riportella, WA2LQQ, President
June 1, 1987

Editorial

by

Robert J. Diersing, N5AHD
Associate Professor of Computer Science
Corpus Christi State University

Introduction

This first issue of *AMSAT-NA Technical Journal* has been in the making for a little more than a year—since March of 1986. As many of you know, the idea was conceived even earlier with the first call for papers having been published in April of 1985. It has taken longer than I hoped to get the first issue in circulation. However, upon reflection, a little more than a year from the time the first material was in hand to final production is not unrealistic.

I will take the liberty to write a longer than usual editorial because there are a variety of topics to be addressed. First, I will review some of the objectives for ATJ. Next will be some commentary on the articles that have been published. Finally, those who have contributed to this issue will be recognized including those who have worked behind the scenes.

AMSAT-NA Technical Journal Objectives

Many professional organizations produce a multitude of technical publications. Large organizations such as the Institute of Electrical and Electronic Engineers (IEEE) and the Association for Computing Machinery (ACM) have at least one technical publication for each special interest group within the respective societies. These publications document the state-of-the-art theoretical and applied work done by the leaders in the fields they represent. For the most part, the very serious work done by AMSAT-NA members has gone undocumented.

Long-time AMSAT members will easily recognize the differences between this publication and both past and current AMSAT publications. A goal of *AMSAT-NA Technical Journal* is to make spacecraft users aware of the tremendous technological challenge associated with the design, construction and operation of modern amateur radio satellites. More importantly, it will be an absolute necessity that this work be documented for certain sources of funds to be exploited for projects like Phase-4.

It is recognized that much of the material presented in these pages cannot be considered easy reading. It is hoped that curiosity will bring satellite users to read ATJ. Speaking from personal experience, I cannot say that I have ever advanced in a technical field without studying material that was completely beyond my level of experience at the time. During the past several years I have participated in a number of forums at ham conventions in Texas. One question that is always asked is, "when are you going to build a geostationary satellite?" Hopefully, ATJ will contain articles describing the engineering considerations for building all types of

amateur radio spacecraft.

Finally, and equally important, we hope to bring you articles from our AMSAT colleagues around the world. This goal is apparent in this issue. With the current level of satellite design and construction activity around the world, articles for future issues of ATJ should be in abundance. Just as amateur radio itself is an international fraternity, so is the group of people who have chosen to specialize in satellite construction and operation. Even when the satellite is primarily the product of a single nation, the technology developed should benefit all AMSAT engineering and user groups.

Contents of this Issue

Consistent with the fact that the first issue should set the tone for future issues, I have tried to include material covering the areas of design, construction and operation. At the same time, I have tried to have activities of several countries represented.

Every spacecraft construction project begins with a conceptual design which must later be refined. Two articles related to the proposed Packet Technology Satellite Experiment-Houston (PTSE-H) project have been included. Gerry Creager, N5JXS, presents the general concepts of the proposed spacecraft. Courtney Duncan, N5BF, shows some of the details of selecting an orbit and spacecraft attitude that will generate enough power for onboard systems.

Since conception and launch of UoSAT-1 in October of 1981, the University of Surrey has been engaged in research in all areas of cost-effective spacecraft engineering and operation. Jeff Ward, G0/K8KA, provides an analysis of the performance of the different types of memory used in the UoSAT-2 Digital Communications Experiment (DCE). Data gathered from experiments such as the DCE is valuable not only to those building amateur radio satellites but to commercial builders as well.

With the launch of Phase-3C still in the future, three articles have been included from our colleagues at AMSAT-DL. Two of them are related to the AFREG 400 bit/s telemetry data demodulator—one describes the operation of the unit and the other gives the alignment procedure. Another article describes a BPSK modulator of the type required for the RUDAK uplink. Finally, Bob McGwier, N4HY, gives the theoretical development of the algorithm used in the Quicktrak program. These four articles show the hardware and software engineering that must be done to support spacecraft in orbit and eventually the amateur satellite enthusiast as end user.

Acknowledgements

I would like to thank all who submitted articles for this premier issue of *AMSAT-NA Technical Journal*. If you submitted an article and it was not published don't give up hope—this is not the last issue. I did not go through this learning process to give up after one issue.

Special thanks go to the authors outside the United States for perservering through the obstacles of working with an editor an ocean away. Werner Haas, DJ5KQ, of AMSAT-DL provided the material that has been reprinted from *AMSAT-DL Journal*. We will be including more articles from AMSAT-DL in the future, especially on RUDAK. Jeff Ward, G0/K8KA, at the University of Surrey also put forth the extra effort to meet my constantly vague deadlines.

Many others have contributed to this publication. The person who has done the most to insure that ATJ

Volume 1, Number 1 made it to press is John Stalmach of the Corpus Christi State University Office of Public Information. John has been a one-man production team and even agrees to do another issue! Text entry and proofreading at many stages was done by my former secretaries Maureen Brown and Ruth Killins. No, they didn't quit because of this project.

I would also like to recognize my wife Julie, the ultimate proofreader. The trained eye of an English/business major who teaches typing is hard to beat. One of her comments along the way was, "I don't know what a magnetorquer is but I don't think it should be spelled three different ways."

Finally, thanks to AMSAT-NA President Vern Riportella, WA2LQQ, for the encouragement and patience required to begin a new project and see it to completion.

An Analysis of UoSAT-2 DCE Memory Performance

by Jeff W. Ward, G0/K8KA

Research Fellow

UoSAT Spacecraft Engineering Research Unit

University of Surrey

Guildford, Surrey GU2 5XH

ABSTRACT

The Digital Communications Experiment payload on UoSAT-2 (OSCAR-11) was designed to provide both a facility for Amateur Radio digital communications and a test vehicle for the hardware and software necessary for large-scale store-and-forward satellite communications. The hardware is being monitored for permanent memory failures, temporary memory upsets and long-term changes in power consumption. This paper presents data gathered during 1985 and 1986 along with some preliminary conclusions drawn from that data.

1.0. The Digital Communications Experiment

The UoSAT-2 mission (conceived in 1983 for 1984 launch) gave several groups of experimenters outside of the University of Surrey the opportunity to get payloads into orbit. One of these groups was the North American AMSAT group working on PACSAT [1]. Early design work for PACSAT had already been done, and flying a small store-and-forward transponder on UoSAT-2 was an ideal opportunity to test hardware and software for use in a dedicated PACSAT satellite.

The resulting small, low-power payload, which was designed, built and tested in only a few months, is the UoSAT-2 Digital Communications Experiment (DCE). The DCE is a store-and-forward communications module built around an NSC-800 microprocessor and 126 kbytes of RAM. It has two asynchronous communications ports which can be connected to any of the UoSAT-2 RF communication channels or the On-Board Computer (OBC).

UoSAT-2 was launched on March 1, 1985 (becoming UoSAT-OSCAR-11), and the DCE was activated in June 1984 to provide an emergency communications link for command of UoSAT-2. A complete store-and-forward operating software system, called MSG2, was put into operation early in 1986, and has seen daily use since then. The structure of MSG2, and details of the use of the DCE to relay Amateur Radio communications are discussed in detail in [2]. The DCE has proven that store-and-forward digital communications from a small satellite to small groundstations is technically viable. But the DCE has another important goal to achieve—the space testing of microcomputer and memory ICs that will be needed to build larger store-and-forward satellite communications systems.

2.0. DCE Hardware

The DCE hardware was designed to meet both the operational and the experimental goals of the payload. The microprocessor, the RAMs and all of the I/O chips are CMOS ICs, resulting in low power consumption which allows the DCE to operate continuously. An NSC-800 processor was chosen because AMSAT had no flight experience with it, and because common Z-80 software development systems can be used to develop code for the NSC-800. UARTs were chosen for I/O because CMOS ICs capable of handling the HDLC protocol were not available, and development time was too short to build an HDLC controller in discrete components (as was done for FO-12).

To provide a wide range of experience with the radiation tolerance and soft-error characteristics of CMOS RAMs, RAMs of several sizes from several makers were used. While this hardware is well-described in [2] and [3], it is important here to clarify the distribution of the memories both within the DCE memory map and on the three PC boards which make up the DCE.

2.1. Memory Map

The DCE memory map is shown in Figure 1. The memory is distributed among three PC boards: the CPU board, the General Memory (GMEM) board and the RAM Unit board. The GMEM board and RAMUNIT board contain only memory ICs and the associated selection and buffering devices. The CPU board also includes the two UARTS, the parallel I/O chip, and the system clock.

2.1.1. PROM

At the bottom of memory (0000-01FF) is the 512-byte Harris 6641 PROM containing the DCE bootloading program. This is a fusible link PROM, and it is provided with an identical backup device. The primary device is functioning correctly, with the bootloader being used to upload all MSG2 software. There has been no need to use the redundant backup. PROM is the only memory on the CPU board.

2.1.2. Harris 2k X 8

Between addresses 07FF and 3FFF are 7 Harris 6564 2k X 8 bit CMOS static RAMS. This is the "general memory" on the GMEM board. Being high-density ICs, these chips are not provided with error detection and correction (EDAC) hardware.

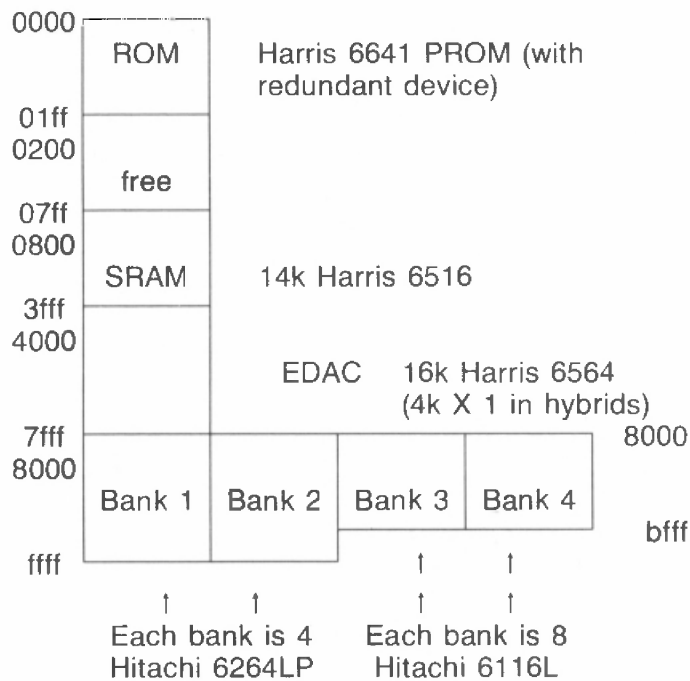


Figure 1. DCE Memory Map

2.1.3. Harris 16k X 4

DCE programs run in the 16 kbytes of memory between 4000 and 7FFF. This is provided by three Harris 6564 ICs. The 6564s are 16k X 4 bit hybrids, each containing 16 4k X 1 memories. Three 6564s are used to provide a 16k X 12 bit memory area; each 8-bit data byte is stored along with 4 bits of Hamming code EDAC information. This Hamming code is a single-bit error correction code. HCMOS EDAC circuits detect, correct and count errors. The EDAC memory and support circuits are on the GMEM board.

2.1.4. Bank-Switched RAM

Current PACSAT plans call for between 4 and 10 Mbytes of RAM to be used for message storage. One method of providing this much memory in the address space of an 8-bit microprocessor is to use bank switching. In the DCE, 96k of RAM on the RAMUNIT board is divided into 4 banks, each of which can be switched into the addresses between 8000 and FFFF. Banks one and two are 32 kbytes, each using 4 Hitachi 6264LP (8k X 8) CMOS static RAMs. Banks three and four are 16 kbytes of Hitachi 6116L (2k X 8) CMOS statics. These RAMs, and the bank switching hardware are on the RAMUNIT board. Banks are selected using the 82C55 parallel port on the CPU board.

3.0. Telemetry

Each of the three PC boards which make up the DCE has a current monitor, the output of which is sampled by the UoSAT-2 telemetry system. The telemetry system, being critical to the mission, is implemented in radiation-tolerant discrete CMOS logic. It periodically samples 60 analogue channels (voltages, currents, and temperatures) and 100 digital status points, formats this information

into checksummed telemetry frames, and transmits the frames. With the telemetry output running at 1200-bits/sec, each channel is sampled once every 4.84 seconds. Telemetry frames can be monitored directly on the UoSAT-2 downlink, or sent to the On-Board Computer (OBC) for further processing. To provide monitoring of telemetry when the satellite is out of range of the UoS groundstation, the OBC can be instructed to take Whole Orbit Data surveys (WOD). Using the standard 4.84 second sample period and 16 kbytes of the OBC memory, a WOD survey results in just under 19 channel-hours of stored telemetry. The OBC can be instructed to survey any combination of telemetry channels. (For extensive discussion of WOD reception and decoding, see [4] and [5].)

3.1. EDAC Counter

Each time the CPU writes a byte in the EDAC memory, the appropriate Hamming error-correction code is calculated and stored along with the data byte. When bytes are read from the EDAC memory, the Hamming bits are used to detect any errors. If an error is detected, the corrected data byte is placed on the data bus and the EDAC counter is incremented. The corrected byte is not automatically re-stored in the memory, and if an erroneous byte is read several times, the EDAC counter will increment accordingly. The stored byte is only corrected when data is read from a location and then explicitly written back to that location. To make sure that a single error is not counted several times before being corrected permanently by a write operation, the DCE MSG2 software includes a memory "washing" routine which periodically reads and writes each location in EDAC RAM. This routine also monitors the error counter as it reads, and if an error is detected, the location of the error is stored in a special DCE message for downloading. To provide an easily received soft-error rate measurement, the DCE EDAC count is transmitted periodically during normal UoSAT-2 DIARY operations. [2]

3.2. Experiments

Using the EDAC counter, the current sensors on the DCE boards, the temperature sensor on an adjacent payload, special programs for the DCE, and the data collection facilities provided by the 1802 OBC, three distinct experiments are being carried out using the DCE hardware:

- 1) Measuring the rate of occurrence of cosmic-ray induced transient errors in the EDAC RAM.
- 2) Logging and characterizing permanent failures in any of the DCE circuits.
- 3) Monitoring the long-term current consumption characteristics of CMOS RAMs and support circuits.

Experimental data collected since late 1985 is presented here along with some preliminary conclusions and plans for further work.

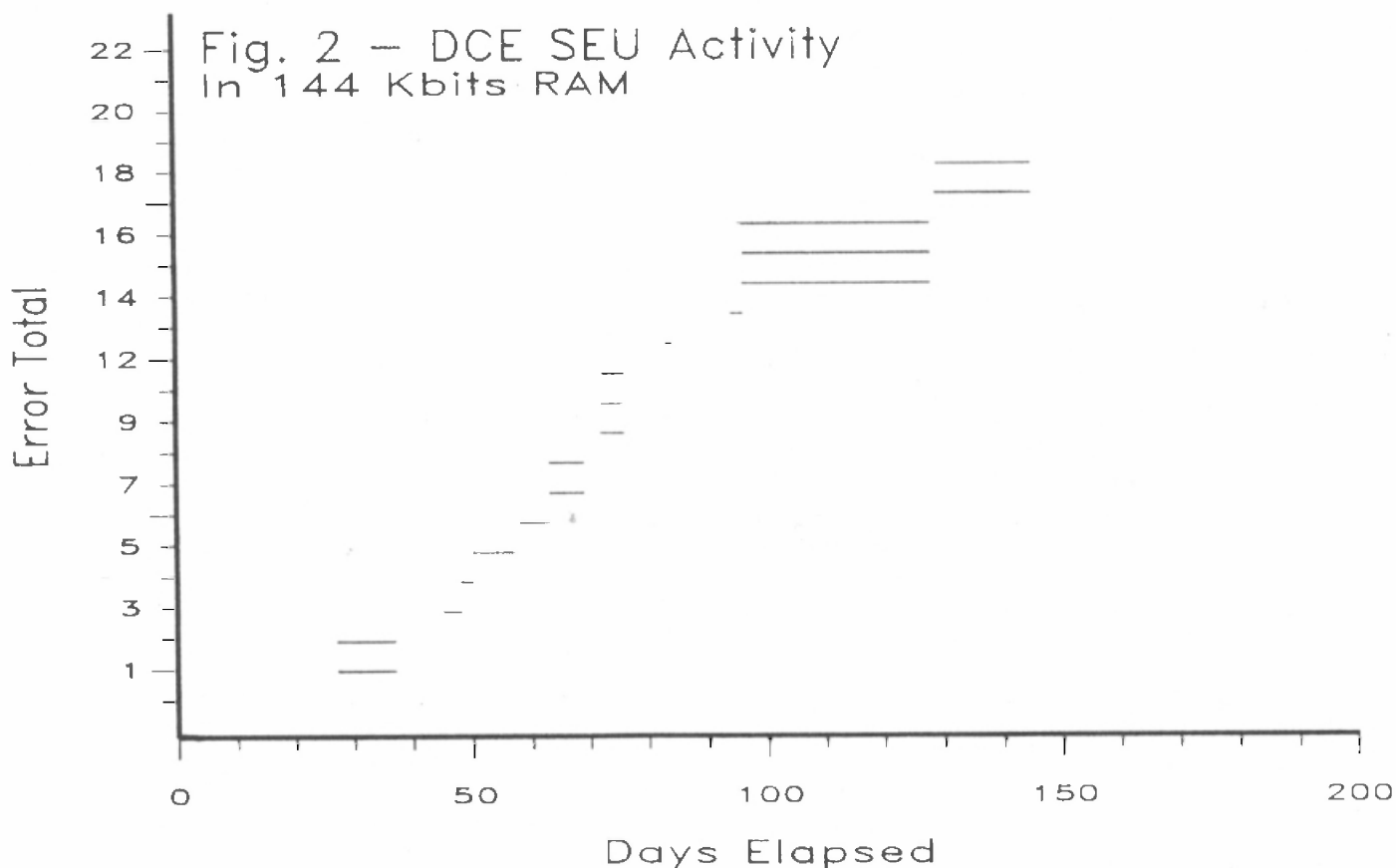
4.0. Soft-Error Rate

When charged particles (cosmic rays) enter the flip-flops which are the memory elements in static RAM, they sometimes introduce enough charge to change the state of the flip-flop, hence the contents of the memory cell. Changes caused in this manner are temporary—the memory can be restored by rewriting it—and so they are called “soft errors,” “transient errors,” or “single-event upsets” (SEUs). While the mechanisms which cause SEUs are fairly well understood, prediction and simulation of the SEU rate for a given satellite payload in a given orbit are very inaccurate. SEU rate depends upon:

- memory device manufacturing technique
- device geometry
- shielding
- satellite orbit
- satellite attitude
- solar activity
- geomagnetic activity.

Thus, reliable simulations and predictions for memory SEU rate for satellites in polar LEO are not available. Results of monitoring the DCE SEU rate (and that in other memories on UoSAT-1 and UoSAT-2) will provide a valuable “calibration” for ground based simulation and testing.

There are 16 kbytes of EDAC memory in the DCE; since each of these bytes is 12 bits wide (to include Hamming information), this makes 192 kbits of memory which can be easily monitored for SEUs. Hard failure of a section of this memory (see below) reduces the active memory to 144 kbits. SEU activity in this memory since September 1986 is shown in Figure 2. This shows 21 errors in 185 days, equivalent to 78.83 errors per day in 100 Mbits of memory (a factor used in other studies of SEU). Figures quoted in [6] are calculated for the worst case, which has the satellite near the poles at the time of maximum solar activity. The prediction is for 5000 SEU/100 Mbit/day with 2.5mm of Aluminium shielding. This figure is reduced to 1000 SEU/100 Mbit/day in less severe conditions. An increase of shielding to 10mm is cited as reducing this figure to 100 SEU/100 Mbit/day. It is interesting to note that the DCE measurements fall far short of both higher figures and much closer to the lower. An analysis of shielding provided by UoSAT module boxes and other spacecraft hardware is being undertaken. Discussions with SEU experts from ESA/ESTEC indicate that there is reasonable correlation between these DCE measurements and ground tests run by ESTEC on similar RAMs.



Note: Each horizontal bar on the graph marks out the range of days during which the corresponding error (read from the y axis) could have occurred. If we had a complete daily record of the EDAC counter, each bar would mark a specific day. Given the incomplete data record, these bars indicate an envelope in which the actual errors occurred and thus provide bounds on error-rate, which is the slope of a line connecting the error occurrence.

Error	Address	Occured Between
1	43E1	06 Oct. - 16 Oct.
2	5E56	"
3	502A	24 Oct. - 27 Oct.
4	7B86	27 Oct. - 29 Oct.
5	5DBA	29 Oct. - 05 Nov.
6	536E	06 Nov. - 11 Nov.
7	54A9	12 Nov. - 17 Nov.
8	531E	"
9	5B09	20 Nov. - 24 Nov.
10	4585	"
11	47A5	"
12	4330	01 Dec. - 02 Dec.
13	4EAB	12 Dec. - 14 Dec.
14	7DF3	18 Dec. - 19 Dec.
15	5408	26 Dec. - 27 Dec.
16	5428	26 Dec. - 27 Dec.
17	7A32	23 Jan. - 26 Jan.
18	4FEF	30 Jan. - 31 Jan.
19	47BC	04 Feb. - 05 Feb.
20		02 Mar. - 03 Mar.
21		06 Mar. - 06 Mar.

Table 1—EDAC errors: 8 Sept. 1986 and 10 Mar. 1987.

The addresses of the SEUs (Table 1) show that each count is a separate incident, and not a multiple detection of a single error. Further, no particular region of memory is more susceptible than any other.

5.0. EDAC RAM Hard Failure

Sometime between orbits #12844 (28 July 86) and #12857 (29 July 86), the DCE EDAC counter began to count up rapidly, recording continuous errors in the memory above 6000 (hex). To find the extent of the memory failure, the DCE memory test program was loaded and run for several days. This program, initially used for ground checkout of the DCE, implements the following test:

- 1) Choose an initial bit pattern and reset the memory pointer.
- 2) Write the pattern to memory at the pointer.
- 3) Read back from that location.
- 4) Check that the byte read is the same as the one just written.
- 5) Check the EDAC counter to see if the read in (4) resulted in a Hamming correction.
- 6) Increment the memory pointer and rotate the bit pattern.
- 7) Repeat 2-6 until all memory has been tested.
- 8) Go through the whole memory re-reading each location, checking the contents (both by watching the EDAC counter and checking the data read against the data written in step 2).
- 9) Go back to step 1.

The initial bit patterns used in step 1 are 00000001, 00000011, 00000111, etc. While this does not result in every possible pattern being written to every location, it provides a thorough test of the memory. Step 8 im-

plements a second pass through the memory, several seconds after the first pass. This identifies memory locations which degrade slowly or as a result of activity in other memory locations. Whenever errors are noted in either pass, an appropriate message is sent on the downlink.

There is no error detection or correction on the messages transmitted by the memory test program, so analysis is based on incomplete record of the data. Nevertheless, programs were developed to filter the thousands of lines of output captured by DCE groundstations and convert the data into a memory map showing bad locations. Two representative maps are shown in Figure 3. These show that the bad locations are limited to a 4-kbyte area between 6000 and 6fff, indicating the failure on one of the 12 memory chips carried on the three Harris Mil Spec 6564 hybrids.

When using patterns with several 1 bits set, most of the locations which fail do so only on pass two. This shows that memory locations which work when written and then read immediately become corrupted slowly or by activity at other locations. Figure 3(a) shows that there are, however, 128 locations (with addresses 6xyz, where x is even, y and z are greater than or equal to C) which fail immediately (during pass 1). And there are other locations (6abc, where a is odd, and bc is less than EC) which never fail. Analysis of this data by the DCE hardware designers may allow further localization of the failure.

5.1. Effects on Current Consumption

Real-time telemetry gathered before and after the failure of the 6564 recorded a marked increase in the GMEM current drain (Table 4b,c). On orbit #12844 it is drawing 34 mA compared to 125 mA on orbit #12857. The telemetry from #12857 was taken while the failed RAM was still being read and written by the MSG2 wash routine, and so it might give high readings for other reasons (logging and correcting the repeated errors increased the amount of writing done by the memory wash routine). However, WOD surveys taken long before and after the incident also show an increase in the EDAC memory current consumption (see below).

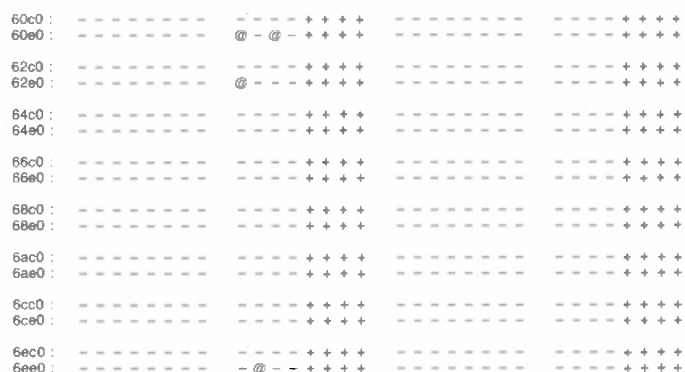


Figure 3(a).

Memory map showing hard failures
in the DCE EDAC RAM
Initial Bit Pattern: 00000000
Bad Memory Range: 60c0 - 6eff

6000	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	- @ @ - @ @ -
6020	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6040	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6060	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6080	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
60a0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
60c0	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -
60e0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	- - @ @ - @ @ -
61c0	- - - - -	- - - - -	- - - - -	- - - - -
61e0	- - - - -	- - - - -	- - - - -	- - - - -
6200	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6220	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6240	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6260	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6280	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
62a0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
62c0	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -
62e0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	- - @ @ - @ @ -
63c0	- - - - -	- - - - -	- - - - -	- - - - -
63e0	- - - - -	- - - - -	- - - - -	- - - - -
6400	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6420	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6440	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6460	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6480	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
64a0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
64c0	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -
64e0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	- - @ @ - @ @ -
65c0	- - - - -	- - - - -	- - - - -	- - - - -
65e0	- - - - -	- - - - -	- - - - -	- - - - -
6600	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6620	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6640	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6660	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6680	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
66a0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
66c0	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -
66e0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	- - @ @ - @ @ -
67c0	- - - - -	- - - - -	- - - - -	- - - - -
67e0	- - - - -	- - - - -	- - - - -	- - - - -
6800	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6820	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6840	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6860	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6880	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
68a0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
68c0	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -
68e0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	- - @ @ - @ @ -
69c0	- - - - -	- - - - -	- - - - -	- - - - -
69e0	- - - - -	- - - - -	- - - - -	- - - - -
6a00	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6a20	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6a40	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6a60	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6a80	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6aa0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6ac0	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -	- - @ @ - @ @ -
6ae0	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	- - @ @ - @ @ -
6bc0	- - - - -	- - - - -	- - - - -	- - - - -
6be0	- - - - -	- - - - -	- - - - -	- - - - -
6c00	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6c20	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6c40	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6c60	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -	@ @ @ - @ @ -
6cc0	- - - - -	- - - - -	- - - - -	- - - - -
6ce0	- - - - -	- - - - -	- - - - -	- - - - -
6dc0	- - - - -	- - - - -	- - - - -	- - - - -
6de0	- - - - -	- - - - -	- - - - -	- - - - -
6ec0	- - - - -	- - - - -	- - - - -	- - - - -
6ee0	- - - - -	- - - - -	- - - - -	- - - - -

Figure 3(b) Memory map showing hard failures in the DCE EDAC RAM.

Initial Bit Pattern: 00000111

Bad Memory Range: 6000 - 6eff

Note: Each -, ☆, + or @ shows the error status of a byte. The address of the first byte in each line is shown on the left. Locations which show "☆☆", indicating failure only during pass 1, must also have failed pass 2, but downlink data showing this was missing.

Key: ☆ = failed pass 1
@ = failed pass 2
+ = failed both passes.

5.2. Effects on DCE Operation

The MSG2 software and all of its tables and memory-allocation links are kept in the EDAC memory. Because of the protection afforded by the EDAC circuits, this memory is crucial to DCE operation. Fortunately, the current version of MSG2 is not long enough to need the entire 16 kbytes of EDAC memory. Indeed, it did not even enter the area which failed. Thus, there is still plenty of room for safe operation and expansion of the MSG2 software. To keep the EDAC counter from counting continuously and obscuring radiation-induced SEUs, the area of EDAC RAM from 6000 to 6FFF is excluded from the MSG2 memory wash routine. Operation of MSG2 has continued without interruption since it was uploaded after the memory test.

It is interesting to note that the failed IC was a Military Specification part, not one of the many standard ICs in the DCE. In a recent article concerning failures of components on AO-10, Karl Meinzer writes "This case (the failure of a MIL spec 2N2907A) has again led to considerable discussion whether it is really wise to use special militarily qualified components ... It is indeed indicative that in all our failures the 'MIL' component are involved, even though we have employed very few of them in our satellites." [7] The DCE experience seems to substantiate these comments.

6.0. Long Term Monitoring

As well as SEUs (the transient effect of cosmic radiation) designers of satellite-borne electronics must be able to predict the long term effects of the total dose of radiation absorbed by satellite electronics. Total radiation dose damages the semiconductor gates which make up ICs, causing increased current drain and device failure. The DCE can play an important role in selection of radiation resistant but inexpensive and dense memory devices for future satellites. To do this, a record of the current consumption of each memory IC is being gathered.

6.1. The "WORM"

Since the current monitors on the DCE measure the current consumption of entire PC boards and not individual ICs, a program was developed which activates a single memory chip while current consumption measurements for that chip are made. The program copies itself from the EDAC memory into another chip, loops in that chip for a predetermined time, returns to the EDAC memory to send diagnostic messages, and then repeats the process for the next memory chip. Because of this action of sliding through the whole memory map, this program is called "WORM." The table of memory addresses and bank switch selections used to tell WORM where to go is shown in Table 2. When WORM is running in DCE memory, the 1802 OBC is instructed to take a WOD survey of the telemetry channels shown in Table 3. The channels other than DCE current channels (14, 15, 16) are included so that changes in DCE current consumption can be checked

against changes in power supply conditions or S/C temperature (the P/W experiment has the closest temperature sensor to the DCE). When sampling 8 channels, the OBC can store 164 minutes of WOD. The WORM program run in 1985 cycled in each chip for 2 minutes, resulting in between 2 and 3 passes through the whole memory during one WOD survey. To increase the number of samples taken in each IC, the WORM time was increased to 4 minutes for surveys taken in 1986.

Static RAM:	0800		
	1000		
	1800		
	2000		
	2800		
	3000		
EDAC RAM:	7000		
Bank 1:	8000	Bank 3: 8000	Bank 4: 8000
	A000	8800	8800
	C000	9000	9000
	E000	9800	9800
		A000 *	A000
Bank 2:	8000	A800	A800
	A000	B000	B000
	C000	B800	B800
	E000		

Table 2—Starting addresses of the chips tested by the WORM program.

Note: Because of permanent failure (detected before launch) at A5F1 in bank 3, the chip starting at A000 in that bank is not used.

No.	Source	Equation
14	RAMUNIT current	$I = (N - 70.4)/6.7 \text{ mA}$
15	CPU current	$I = (N - 187.1)/2.0 \text{ mA}$
16	GMEM current	$I = (N - 121.3)/2.1 \text{ mA}$
21	+ 10 V line current	$I = 0.97N \text{ mA}$
22	+ 10 V PCM voltage	$V = 0.015N \text{ V}$
41	+ 5 V line current	$I = 0.97N \text{ mA}$
42	+ 5 V PCM voltage	$V = 0.0084N \text{ V}$
48	P/W temperature	$T = (480'N)/5 \text{ C}$

Table 3—Telemetry channels included in WORM WOD surveys.

6.2. WOD Plots

The WOD plots in Figures 4-6 are scaled in telemetry counts up the Y axis. Conversion equations from counts to engineering units for the three DCE current channels are shown in Table 3. The marks on the X axis are roughly calibrated, and divide the graph into 10 equal time segments. The legend above each plot tells which survey it came from, the offset of the first and last telemetry samples displayed (measured from the start of the survey), and the average telemetry value for the entire plot.

6.3. RAMUNIT Current

Figure 4 shows RAMUNIT current as measured during the two surveys. (The X axis of the early survey has been expanded so to make up for the 2:1 difference in WORM looping times.) The average current drain was 16.4 mA during the first WORM and 15.5 mA during the second, indicating that there has been no great degradation of the CMOS static RAMs in the RAMUNIT. Different chips clearly show different current drain, with the lowest consumer the 6264 at C000 in bank 2 and the highest the 6264 at A000 in the same bank. The current drain of the RAMUNIT memory during the WORM program has a very distinctive "signature," which does not change from survey to survey. The 6116 ICs in banks 3 and 4 seem to vary much less than the larger 6264 parts in banks 1 and 2. Other than this, there is no clear differentiation among the four banks.

6.3.1. Anomalies

This would be a clear and understandable record of RAMUNIT current if it were not for the two "spikes" in the data. The earlier, larger transient occurs when the WORM program is looping in the chip at address 0800 on the GMEM board. The second occurs when WORM activity should be at 7000, in the EDAC memory on the GMEM board. Figure 5 is an expanded display of the first spike, showing each of the WOD samples. It rises for 25 seconds and then takes nearly 2 minutes to fall to a quiescent value. This could be the charging current characteristic of a large capacitive load, or it might be a fault in the current measurement system. I have not been able to identify such a large capacitive load on the RAMUNIT board, let alone one which is linked to address 0800 or 7000. It is highly unlikely, however, that these are artifacts of the telemetering process. Discussions with Dr. L. Mansi, the telemetry system designer, revealed that there are no large capacitive elements in the current monitors, the telemetry multiplexing system or the ADCs. Also, the rapid fall in current as the WORM leaves bank 2 chip A000 is correctly measured by the telemetry system. I will study this problem further through specialized programs for the DCE and experiments with the DCE simulator at UoS. This problem is aggravated by the lack of complete documentation for the DCE RAMUNIT.

6.4. GMEM Current

The GMEM current measurements (Figure 6) are confused by a problem similar to that uncovered on the RAMUNIT. In all but one case, the 4-minute WORM period which should show the current consumption of a single IC is obscured by a transient which starts at the beginning of the period. The beginning of each period includes 2 events:

- 1) Transmission of a short message through a UART on the CPU board.
- 2) Copying of the WORM loop from 4000 (in the EDAC RAM) to the next memory chip.

Why these actions should cause current transients on the GMEM board is unknown, as is why such transients should take minutes to decay.

6.4.1. EDAC RAM Current

The one chip which can be seen clearly in the GMEM current measurements is the EDAC RAM. This is the single flat area in the survey. Data from the first WORM run shows current consumption in this area as 33.5 mA, during the second survey the value is 54.1 mA, and a special survey which placed the WORM in the failed memory region (at 6000) showed an average of 68.95 mA. (Table 4 a, d, e) This indicates that the EDAC RAM started drawing more current at the time of failure, and that it is the bad portion of the IC (or ICs) which is responsible for this. There seems to be no consistent correlation between GMEM current consumption and its temperature, indicating that the GMEM current sensor is not affected by temperature.

6.5. WOD and WORM Conclusions

Until the source of the glitches in RAMUNIT current, and the causes of the long time constants shown in both RAMUNIT and GMEM current are located, detailed conclusions should not be drawn from the WORM WOD. Some broad, but useful, observations can be made:

- In the months between the two surveys, current drain by RAMUNIT memory ICs (6116 and 6264) has not increased.
- The failure of one or more 6516s has resulted in increased EDAC RAM current consumption, even when the bad memory area is avoided.

The first point is a sign that these chips are space worthy, at least for their first two years. The second indicates that in large areas of memory, in which current consumption must be kept down and failures are probable, there should be some mechanism for completely isolating damaged ICs from the power and computer buses.

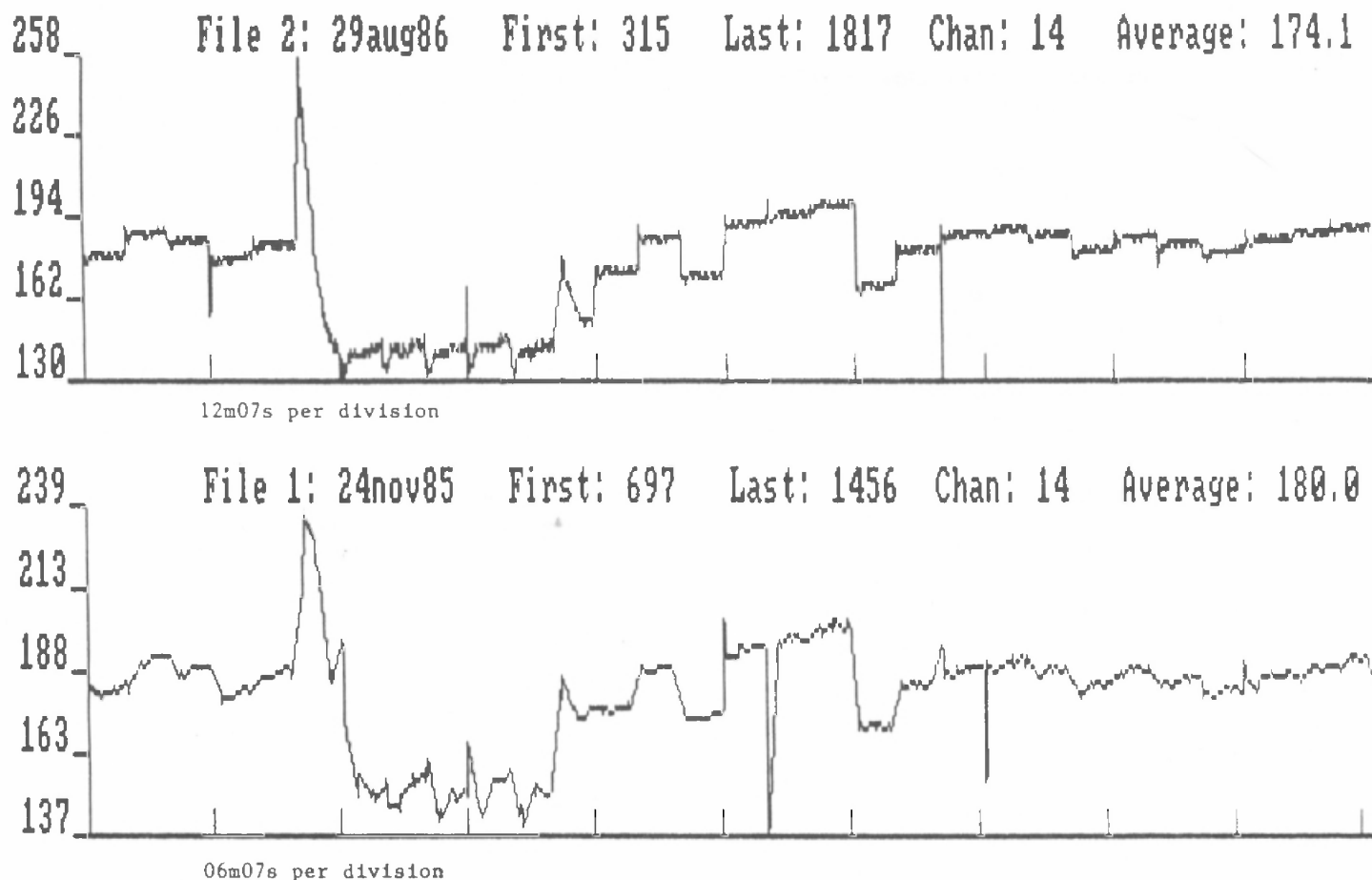


Figure 4. DCE RAMUNIT Current Consumption

7.0. Further Investigations

To make best use of the DCE as a test bed for satellite hardware, the surveys of SEUs and total-dose degradation must continue reliably. We must find the cause(s) of the transients and long decay periods shown in WOD surveys, and if these cannot be avoided, the WORM program must be supplemented by programs which allow correct measurement of current consumption on the GMEM board.

Error detection and correction in the RAMUNIT memory has received little attention. Once proper software is written, this 96 kbytes of high-density RAM will provide invaluable data concerning the frequency and characteristics of SEUs in large CMOS memories. We plan to develop an EDAC scheme, based on an appropriate block code, which can run without interfering with the operation of the MSG2 software.

Results from all of these experiments will be important input to the design of UoSAT-C. Plans now call

for this satellite to carry both a large (c. 10 Mbytes) "RAM disk" for shared use by all onboard processors, and a store-and-forward packet payload serving the PACSAT goals. Both of these payloads will depend on reliable operation of large memories, and successful detection and isolation of failed hardware. The MSG2 experiments will help UoSAT-C software designers, and the DCE hardware monitoring will result in more robust spacecraft memory hardware systems.

8.0. Acknowledgements

Thanks are due to Bob Diersing and the students who operate the Corpus Christi State University UoSAT Receiving Station for providing their archive data to the author. This was the only source of 1985 WORM data and telemetry from the orbits immediately surrounding the hard RAM failure. Harold Price, NK6K, provided most of the data used to generate the memory failure maps. A complete list of those involved in the DCE project appears in [2].

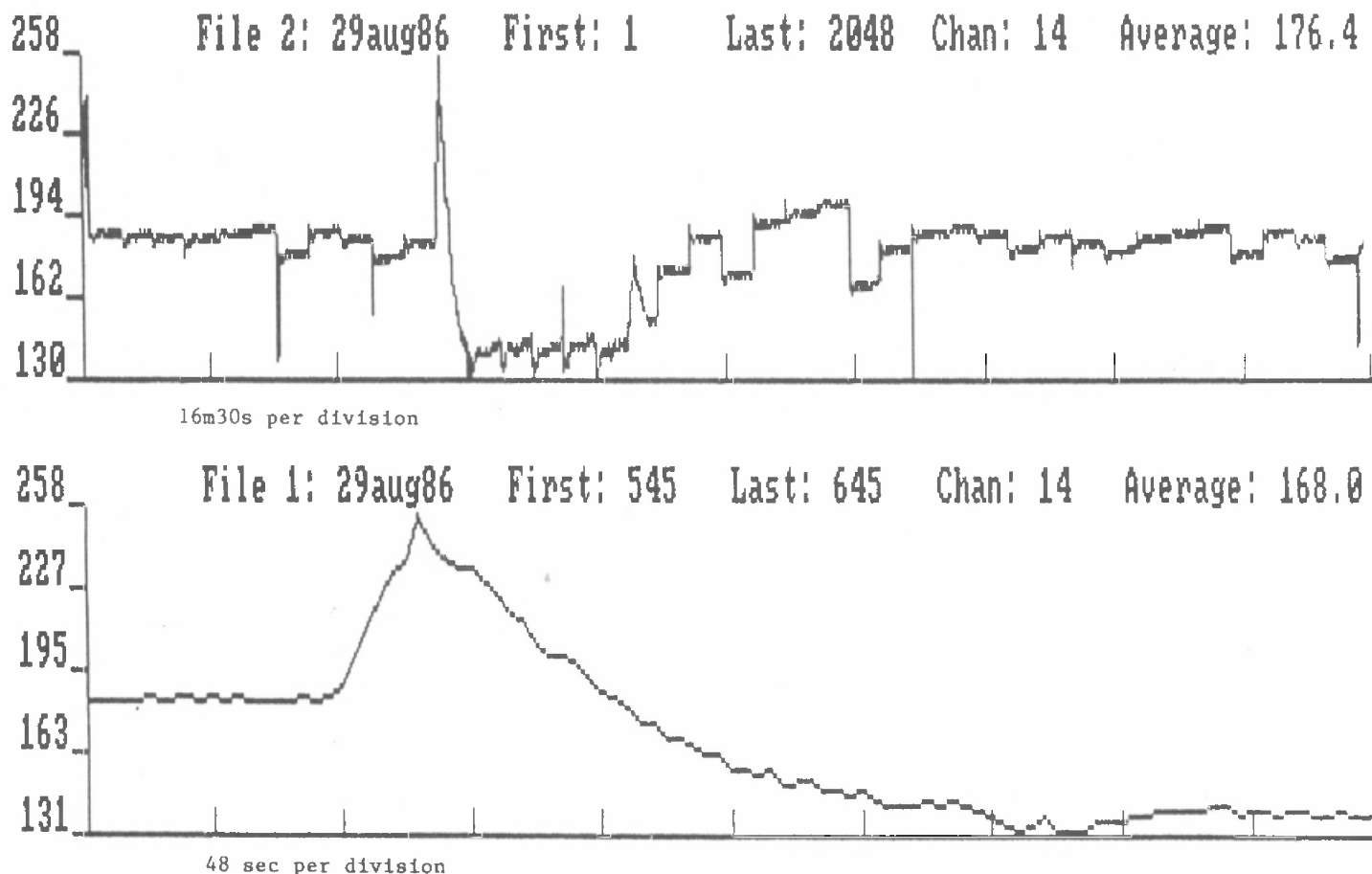


Figure 5. DCE RAMUNIT Current Showing Expanded 'Glitch'

Note: Lower graph is an expanded display of the event which starts at 45m25s on the upper graph.

Bibliography

- [1] "The PACKSAT Project," D. Connors, *Proceedings of the Second ARRL Amateur Radio Computer Networking Conference*, ARRL, 1983.
- [2] "The UO-11 DCE Message Store-and-Forward System," J. Ward and H. Price, *Proceedings of the Fifth ARRL Amateur Radio Computer Networking Conference*, ARRL, 1986.
- [3] "The OSCAR-11 Packet Experiment," L. Johnson, *Proceedings of the Third ARRL Amateur Radio Computer Networking Conference*, ARRL, 1984.
- [4] "Processing UoSAT Whole-Orbit Telemetry Data," R. Diersing, *Proceedings of the 4th Annual AMSAT Space Symposium*, AMSAT-NA, 1986.
- [5] "UoSAT-OSCAR-11 Spacecraft Data Formats," S. Holder, *UoSAT Spacecraft Data Booklet*, University of Surrey, 1986.
- [6] "MAILSTAR Mission Study," Dr. M. Sweeting, et. al., University of Surrey, 1985.
- [7] "Three Years of Operation with AMSAT OSCAR-10," K. Meinzer, *AMSAT/DL Journal*, 1986.

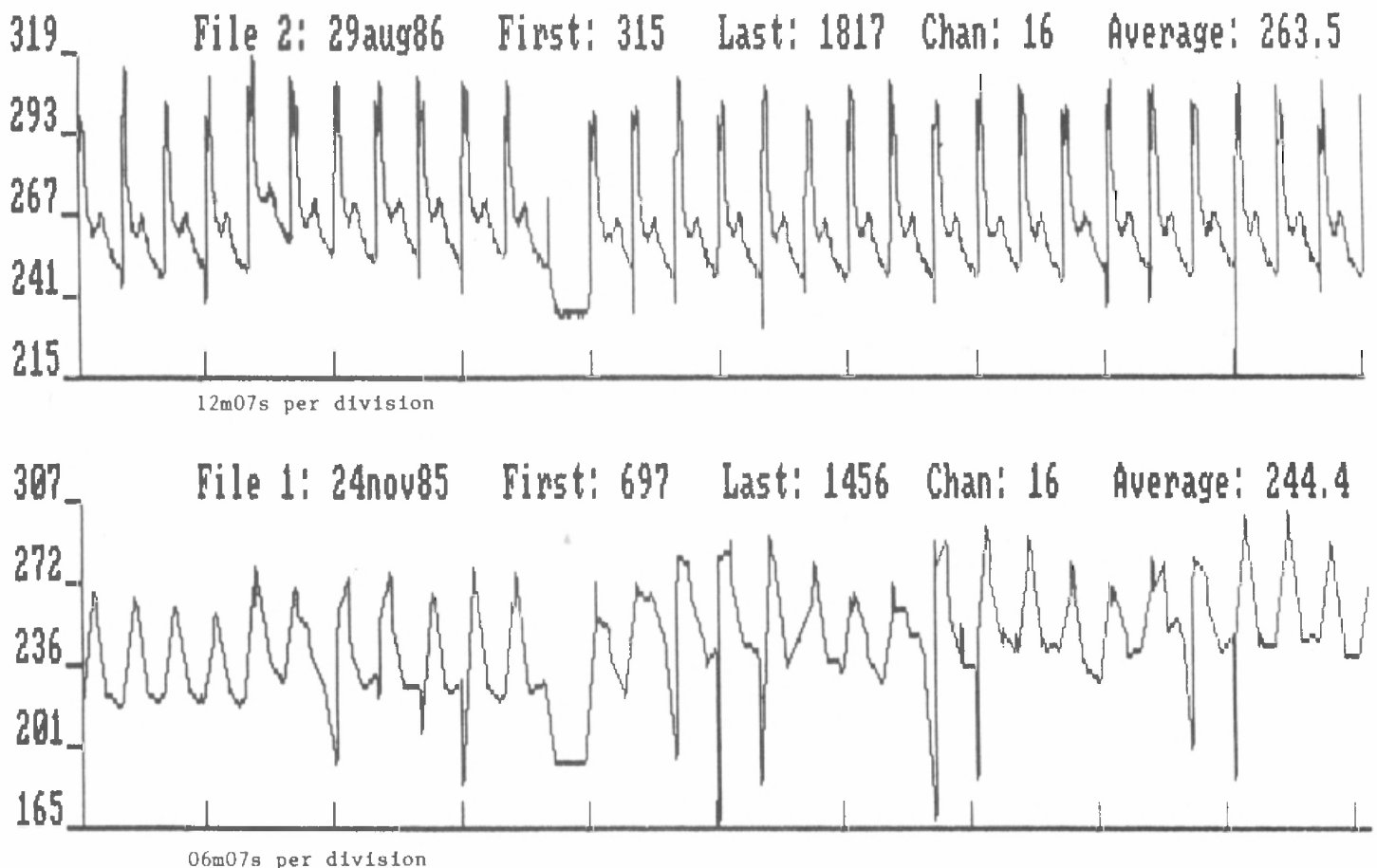


Figure 6. DCE GMEM Current Consumption

A Look at the Phase-3C Spacecraft

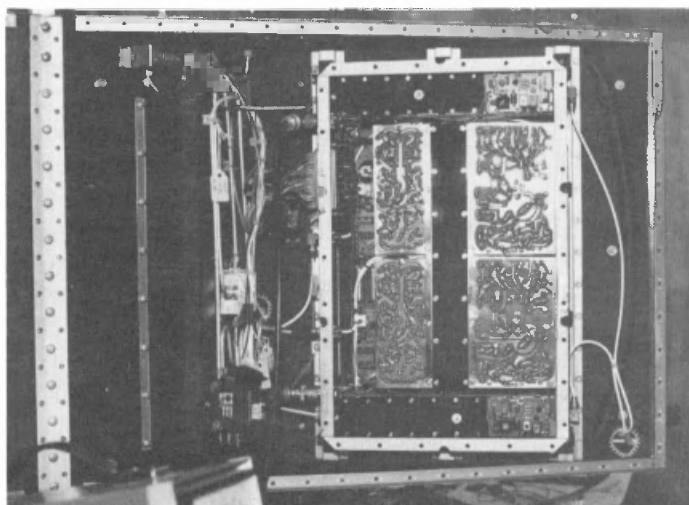
Robert J. Diersing, N5AHD
Editor, AMSAT-NA Technical Journal

by **Jan King, W3GEY**
and Vice President for Engineering, AMSAT-NA

In May of 1986, the editor had the opportunity to visit the AMSAT laboratory during the final integration of modules for the Phase-3C spacecraft prior to thermal vacuum testing. It was quite an experience to observe the work of all those involved over the period of several days. It was also a pleasure to have met Dr. Karl Meinzer, DJ4ZC, Phase-3C project head, other the members of the AMSAT-DL team, and all of the

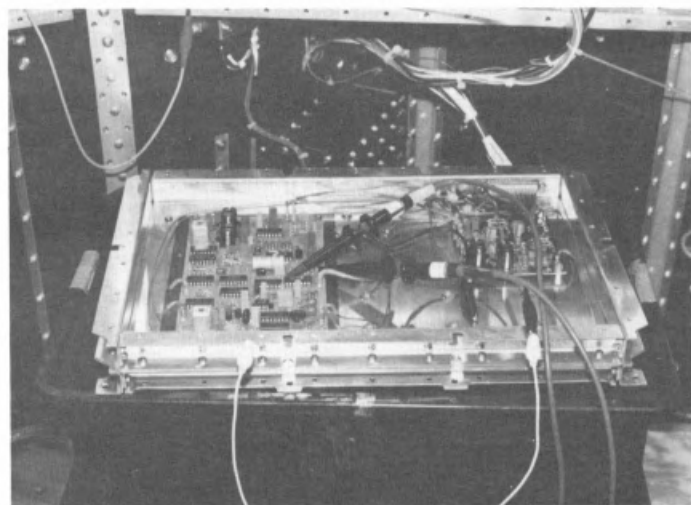
amateur satellite enthusiasts from the Colorado area.

During the visit a number of pictures were taken. Although various pictures of spacecraft appear in AMSAT publications, it was thought that our readers would find a complete set of photographs of Phase-3C interesting. The commentary on the contents of each photograph has been provided by Jan King, Phase-3C project manager.



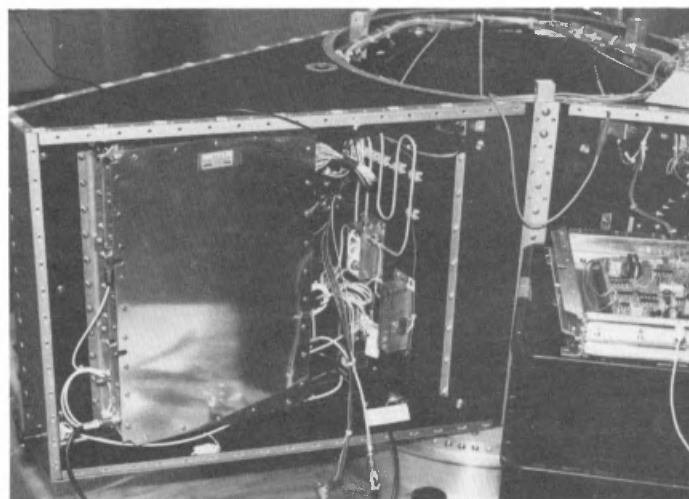
Left side: Relay panel and three-way power splitter for two meter antenna system.

Center: Transmitter module containing 2 meter and 70 centimeter HELAPS (High Efficiency Linear Amplification through Parametric Synthesis) transmitters.



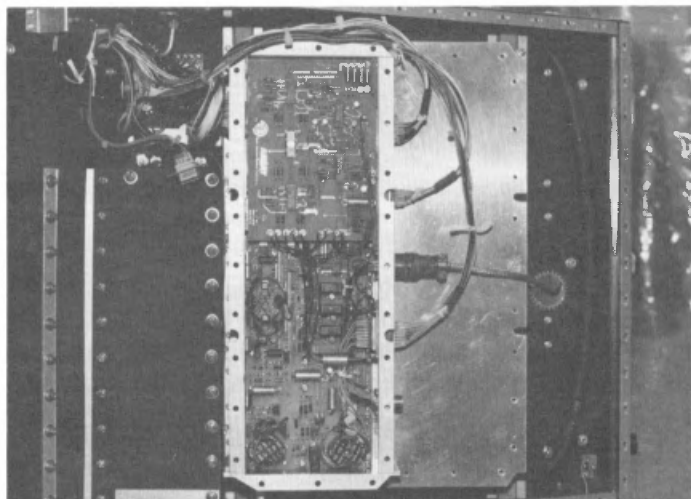
RUDAK packet radio transponder 2400 BPS PSK demodulator under test prior to integration into the spacecraft.

Behind RUDAK inside the spacecraft the top of the main battery box can be seen.



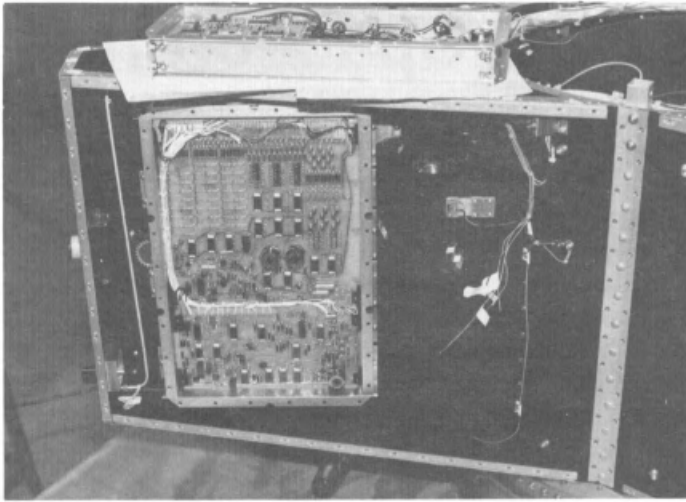
Center: Module containing the Mode B and Mode J/L receivers. One is stacked on top of the other.

Right center: Another relay panel with three-way power splitter and omnidirectional antenna diplexer.



Left side: Box contains 10 AH primary battery pack.

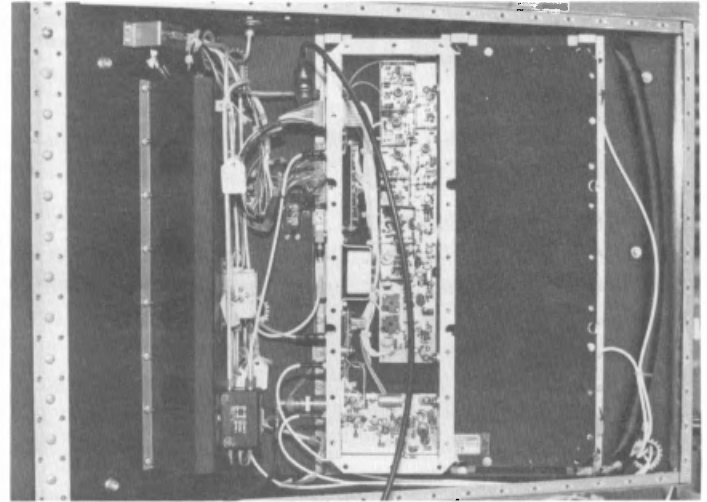
Center: Open module is the Liquid Ignition Unit (LIU) which is mounted on top of the RUDAK transponder.



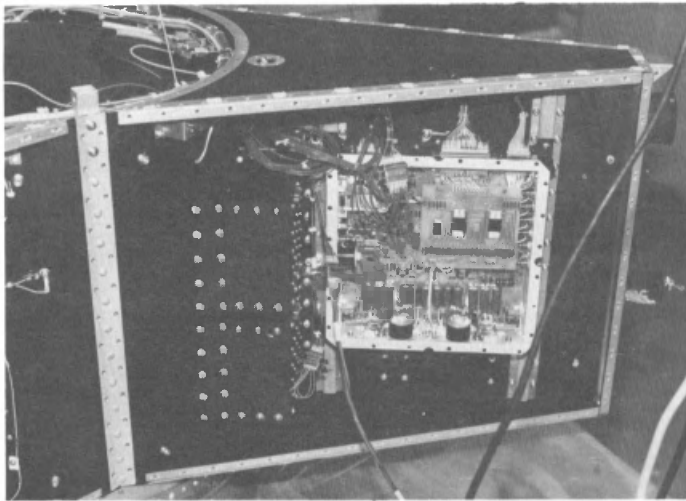
Left arm end: Small black box at center of arm is the SAFE/ARM assembly for the kick motor. Small box near bottom of arm is feed point for 2 meter antenna.

Left center: Integrated Housekeeping Unit (IHU) module. To the right of the IHU (not very clearly visible) is the Helium bottle. Unconnected wiring is for temperature and pressure telemetry.

Sitting on top: Liquid Ignition Unit (LIU) kick motor firing electronics module.



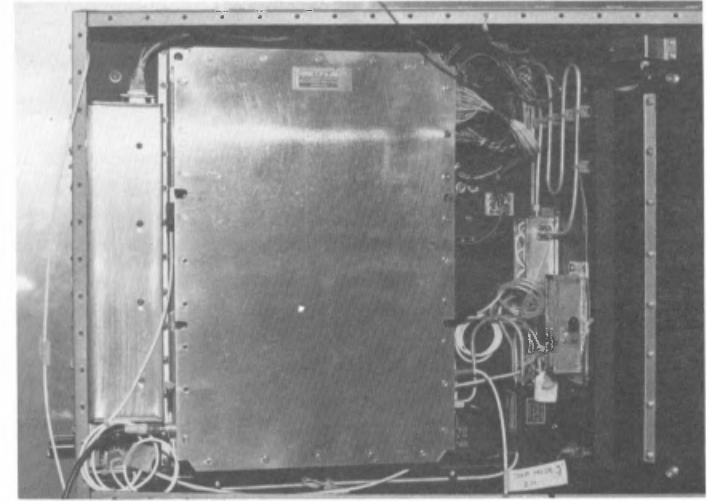
Center: Mode-S transponder IF unit mounted on top of Mode B and Mode J/L transmitter module.



Left side: Two auxiliary batteries.

Center: Battery Charge Regulator (BCR) module. Small hole in top is for 70 centimeter high gain antenna. Tubing for carrying motor fuel to the kick motor can also be seen at the perimeter of the larger center hole.

Right side: Curved tube is one of three nutation dampers.



Left side: Mode-S transmitter mounted between end of arm and Mode B and Mode J/L receiver modules.

BPSK Modulator for RUDAK Operation

by

Knut Brenndoerfer, DF8CA

Lindenstrasse 2, D-8045 Ismaning, West Germany

(Reprinted from *AMSAT-DL Journal*, Vol. 13, No. 5)

(Translated by Don Moe, DJ0HC/KE6MN)

RUDAK is accessed in the 24cm band at 2400 Bit/s, whereby the carrier must be bi-phase modulated. The data signal is also differentially encoded prior to modulation. Since not everyone is familiar with these techniques and concepts, a universal BPSK modulator will be described in the following article and the corresponding concepts explained. The modulator can be reproduced with little effort and can BPSK modulate any carrier between 5 to 500 MHz having a level of +3 dBm.

Modulation means applying information to a carrier. In the case of AM for example, the amplitude of the carrier is modulated with speech; for FM, the frequency of the carrier is varied slightly according to the speech. As computers become more widespread, the demand for means to transmit digital information by radio increases. While the established modulation type, FM, was modified (FSK) for digital transmission for RTTY, for example, this method quickly reaches its limits in satellite operation. Since the optimal usage of transmitter power is foremost, a significantly more effective type of modulation was found in digital phase modulation, which permits perfect demodulation even for very weak signals. The comparison to synchronous FSK is approximately 4 dB, meaning a reduced power requirement by a factor of 2.5. (1)

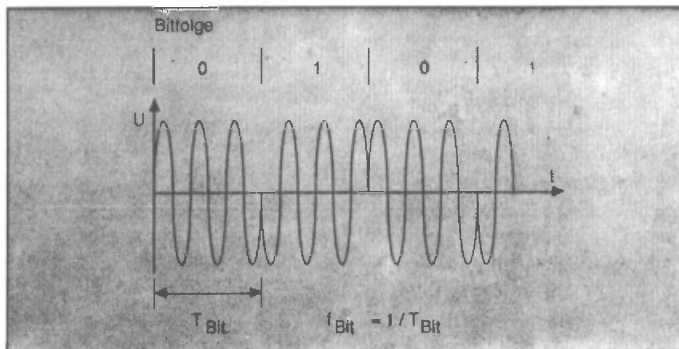


Figure 1—BPSK modulated sine-wave carrier in the time domain.

The appearance of a phase modulated signal in the time domain, as it would be observed on an oscilloscope, for example, is shown in Figure 1. It can readily be seen that the sine wave carrier oscillations do not change their frequency; the carrier is shifted 180 degrees in phase,

thus inverted, depending on the digital signal. The frequency spectrum of a carrier bi-phase modulated with a 400 Hz square-wave signal is shown in Figure 2. With a bit of imagination it can be seen that the spectral envelope has the typical “(sin x)/x” pattern of most of the digital modulation methods and that the carrier is suppressed, and hence not transmitted. This is most noticeable during the construction of a demodulator, since a certain effort has to be expended to reconstruct the non-existent carrier. (2) Additional details about phase modulation and other digital modulation methods can be read in (3).

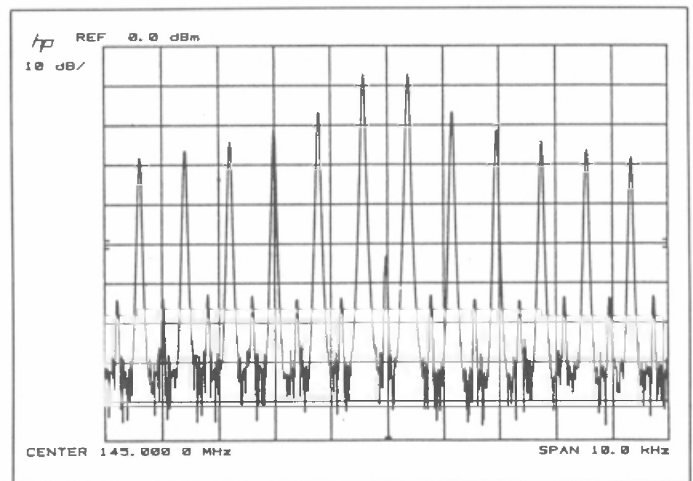


Figure 2—Frequency spectrum of a carrier bi-phase modulated with a 400 Hz. square-wave signal. Photo center corresponds to 145.0 MHz. with ± 5 KHz. displayed. Vertical scale is 10 dB per line.

There are many possible ways to generate a BPSK signal. The direct method is to modulate a 24cm carrier. It sounds quite difficult to modulate a 1.2 GHz carrier directly, but in practice a modulator can easily be built using strip line techniques. Figure 3 shows the schematic for such a modulator. A 90 degree ring hybrid with two PIN diodes is used. The diodes are only switches: with current they are effectively a short circuit, without current they essentially do not exist at the high frequency. The phase angle of the RF signal is inverted through the common switching of the diodes on and off. In practical implementation however, expensive Teflon

circuit board material must be used, and the mechanical dimensions should be maintained more exactly than is possible with amateur methods. A sample design built with inexpensive FR4 epoxy material resulted in a phase error of approximately 40 degrees due to the wildly varying dielectric constants (which should be called variables instead). An additional defect in this type of modulator is the amplitude change of up to 1.5 dB from one phase angle to the other, caused by different signal paths for On and Off and by the losses in the conducting PIN diodes. For these reasons, the version of the modulator has been put aside as second best. If anyone is interested in it however, this modulator can also be published with construction guidelines; please inform AMSAT/DL or the author.

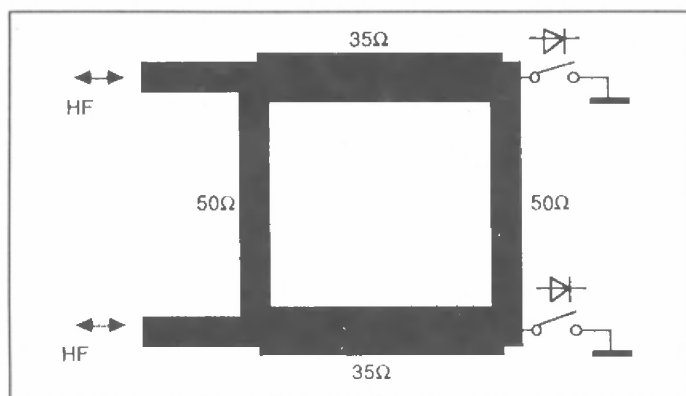


Figure 3—Schematic for 24 cm. BPSK modulator implemented as strip line circuit with RF chokes on the DC supply leads.

Recognizing that the carrier is only switched back and forth between normal and inverted modes in BPSK modulation, any mixer stage can thus be used as a BPSK modulator. Special Schottky-diode ring mixers are ideally suited for this, since they are available as finished modules. The prices could be lower and the drive level higher, but these problems can be circumvented if necessary. Figure 4 shows the basic construction of most of the available Schottky-diode ring mixers, as they are marketed for example under the type designations: HPF505, IE500, SRA1, MD108, etc.

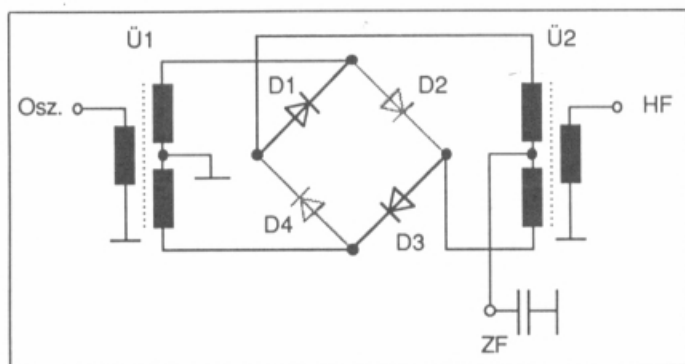


Figure 4—Basic construction of most available Schottky-diode ring mixers.

The switching action in the mixer is initiated by feeding positive or negative current into the IF input. The diodes are then driven as switches. If a current flows in the forward direction through the diodes, they become conductive for RF. If the diodes are reversed biased, no current flows, blocking the diodes for RF also. Current flowing into the IF input passes through D1 and D3 to the ground, thus connecting the high side of T2 with the high side of T1 via D1, and both low sides of the transformers via D3. The diodes D2 and D4, marked with dots, are blocked. If the current in the IF input reversed, D2 and D4 become conductive and connect both transformers diagonally. Compared with the prior condition, this causes a 180 degree phase shift in the output signal, thus giving BPSK modulation.

The positive side is that even the cheapest mixers are usable in the range from 5 to 500 MHz. On the minus side however, the RF carrier is attenuated 3 dB, and mixers in a normal configuration (+7 dBm LO) can only pro-

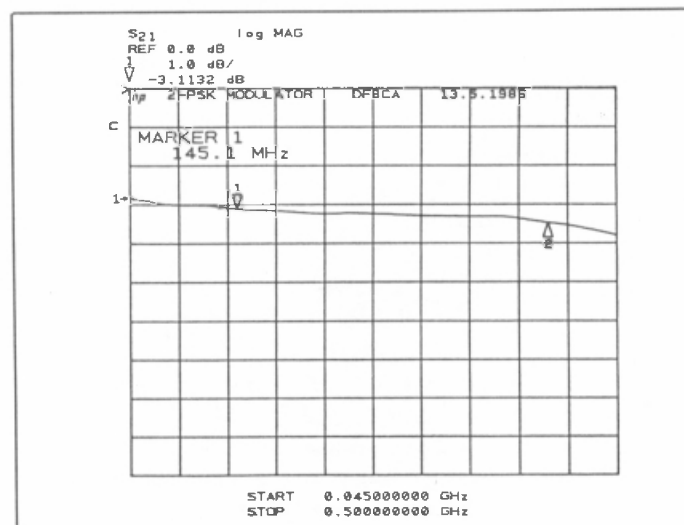


Figure 5—Attenuation of the sample design between 45 and 500 MHz. Vertical scale is 1 dB per line.

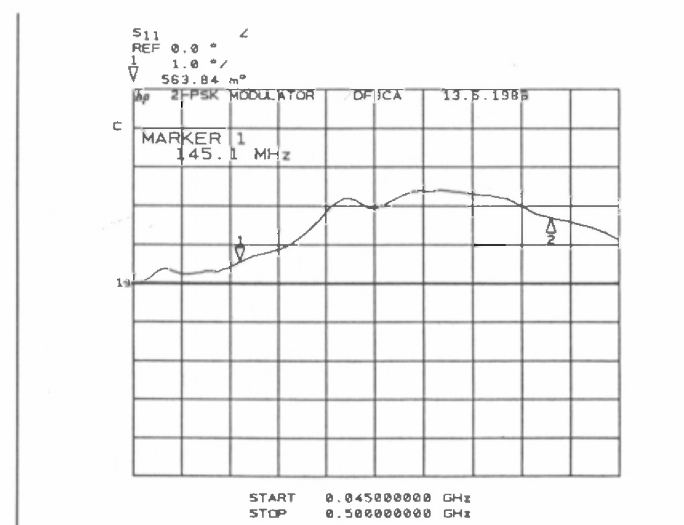


Figure 6—Phase error of the sample design from the ideal 180 degrees. Vertical scale is 1 degree per line.

A small circuit board was designed as shown in Figure 8, and the components are installed according to Figure 9. The circuit board fits into a commonly available tin-plated box having the dimensions 74 x 37 x 30mm. The module is now ready for installation. There are almost no limits on the imagination at this point. With little effort the modulator can be installed in the 23cm transmitting converters or transverters from SSB Electronic. My modulator is in a LSM 24 transmitting converter. Since the models LT23S and USM3 have a similar or even identical circuit at the corresponding location, installation in these should also be quite easy.

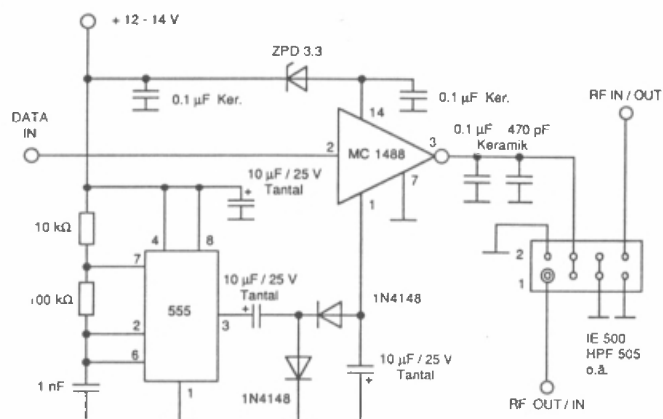


Figure 7—Schematic of the broad-band BPSK modulator.

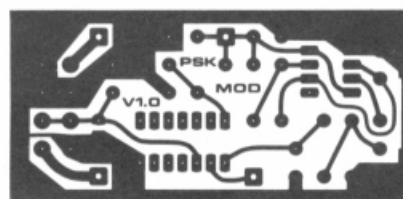


Figure 8—Circuit board layout of the BPSK modulator.

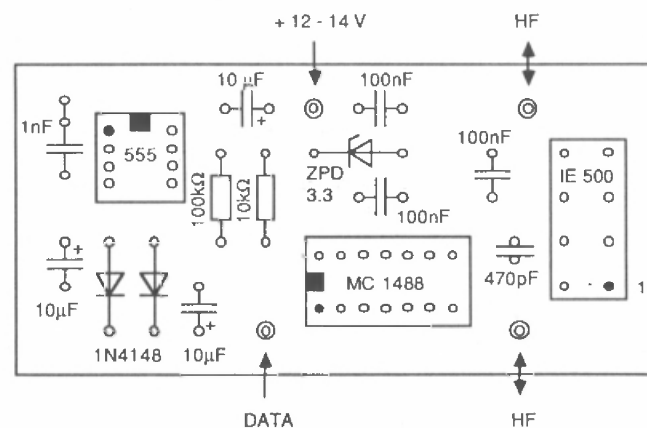


Figure 9—BPSK modulator parts placement.

The excerpt from the schematic (Figure 10) shows the 2m input section of the transmitter mixer. The 2m signal is attenuated at first and then passed symmetrically via a balun to the two mixer transistors. Prior to this balun, either a formed coil or a toroid, the signal path can easily be opened up to feed the 2m carrier to and from the modulator via two thin Teflon coax lines. In order to assure a good ground connection, the lines should be soldered to the upper side of the circuit board and then routed through holes and small exposed rings in the grounding surface to the ends of the separate traces. There is adequate space in the prefabricated equipment for the modulator and also the digital input connector. The power can be supplied from the transverter.

The 3 dB attenuation of the modulator can be easily compensated with the attenuator potentiometer for the input transmit signal. In my LSM24, the level of the 0.5 Watt 2m signal was at -13 dBm at the balun input, hence the modulator must be fed at -10 dBm. These levels are therefore more than 10 dB below the maximum possible drive level.

The digital drive to the modulator can come from various sources. For RUDAK operation, a TNC2 and a TNC1 with modified WA8DED software are suitable. Unfortunately, signals incorrectly encoded for RUDAK operation are supplied by the TNCs' modem connectors. However, DB2OS is publishing a small circuit board, which can easily convert all digital signals used in amateur satellite operation (RUDAK, JAS-1, AMSAT telemetry).

In a following issue, an article will describe connecting the BPSK modulator to the 23cm transceiver IC1271, without internal modification, thereby not affecting the valuable guarantee. Additionally, a "home-made mixer" is under development, which should raise the drive level of the modulator to 100 mW, approximately 20 dB.

- (1) Dr. Karl Meinzer: "Die digitale Nachrichtentechnik der AMSAT Phase-III Satelliten." (Digital telecommunications in AMSAT Phase-III satellites.) *CQ/DL*, Issue 10/1978, page 447-453.
- (2) Dr. Karl Meinzer, DJ4ZC, Heinz Moelleken, DL3AH, and R. Verroen: "Satelliten-Telemetrie-Interface fuer 400 Bit/s." (Satellite telemetry interface for 400 Bit/s.)
Heinz Moelleken, DL3AH: "Abgleichanleitung der AFREG-Platine." (Alignment instructions for the AFREG board.) *AMSAT/DL Journal*, Nr. 3, May/June 1986, page 4-8.
- (3) Rudolf Maeusl: "Digitale Modulationsverfahren." (Digital modulation methods.) Dr. Alfred Huethig Verlag, Heidelberg, 1985 ISBN: 3-7785-0913-6.

Satellite Telemetry Interface For 400 bit/s

by Karl Meinzer, DJ4ZC
H. Moelleken, DL3AH
and R. Verroen

(Reprinted from *AMSAT-DL Journal*, Vol. 13, No. 2)
(Translated by D. Moe, DJ0HC/KE6MN)

Abstract

The following is a description of the circuit used to receive the 400 bit/s telemetry data sent by OSCAR-10 and the packet radio data to be sent by RUDAK after its launch towards the end of the year.

Data Modulation Method Used by AMSAT

The AMSAT satellites utilize so-called phase-shifted keying as modulation for the transmissions of digital data. When the radio link is limited in its capabilities due to noise, phase-shifted keying (PSK) provides a solution requiring the least transmitter power. For this reason, it was selected for the Phase-3 satellites and subsequently also for RUDAK. A more complete substantiation for PSK was published in *CQ-DL* (October 1978). That article also describes the standards, as settled upon for the Phase-3 satellites; here only the more important points will be reiterated.

The phase of the carrier can take on two conditions, 0 or 180 degrees depending on the data. Since both conditions are equally probable, no carrier is actually present, only the sidebands of the data. In order to simplify the recovery of the data's clock signal, the phase is not directly modulated with the data, rather the data is exclusive-OR combined with the clock (the clock is presumed to have a 50% duty cycle). Additionally, the data bits themselves are not used for the modulation; rather, a logic circuit generates a new data stream (T), in which the difference between adjacent data bits (0 or 1) describes the contents of the data. When two adjacent

bits are different, a 1-bit is sent. If the adjacent bits are the same, a 0-bit is sent. Figure 1 illustrates this procedure. Since the phase can only be recovered in the receiver with a 180 degree ambiguity, the possibility of the data coming out of the receiver inverted is thereby prevented. (The possible ambiguities of the signal will be discussed again later.)

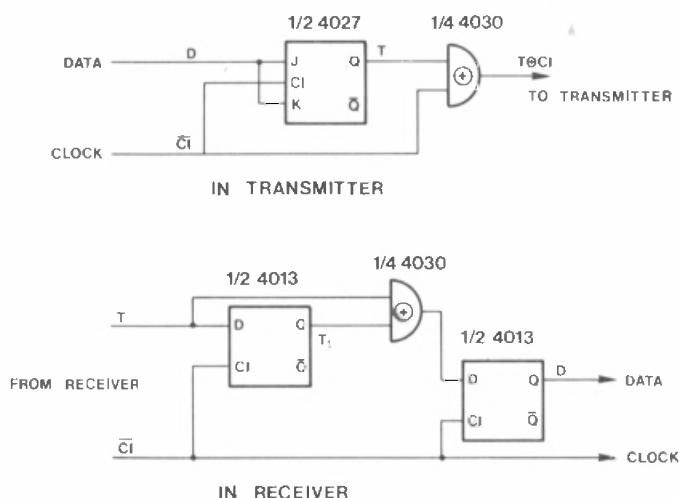
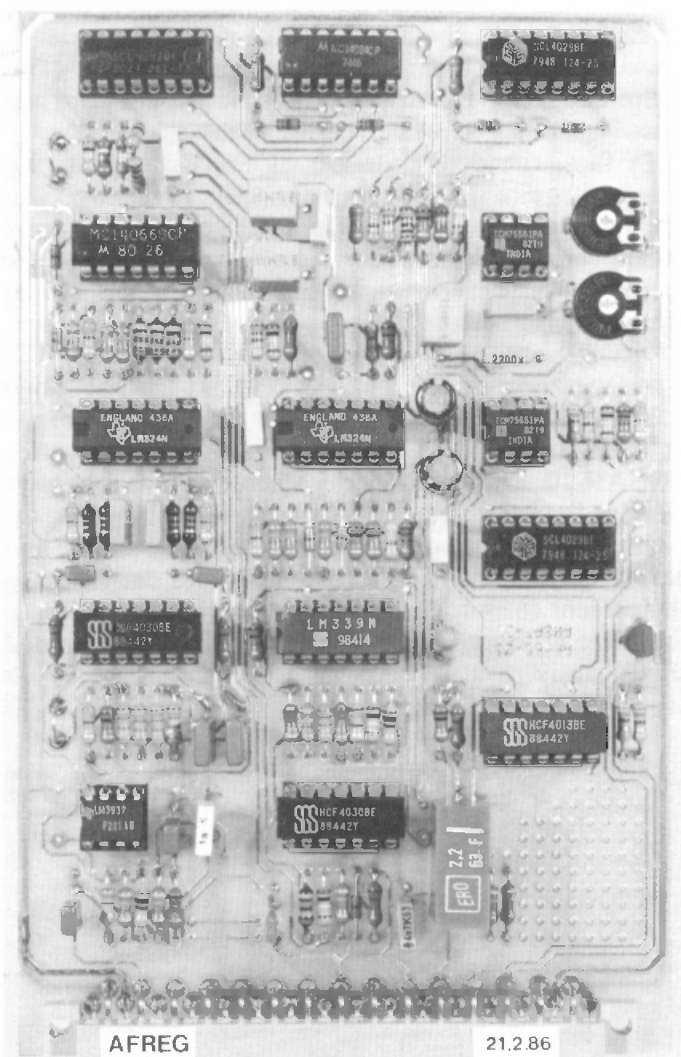


Figure 1 — Differential biphase encoding and decoding.



For the satellite's data transmitter, a data rate of 400 bit/s was elected. Using the previously described modulation, this means that the band width of the transmitted signal corresponds approximately to the width of a SSB channel (about 2 KHz).

Reception of PSK

For the reception of these data transmissions, the use of a SSB receiver is recommended. The audio frequency output from the receiver, with a middle frequency of about 1500 Hz, corresponds to the transmitted signal, which was mixed down to this "intermediate" frequency. In order to recover the data, it is necessary to demodulate this 1500 Hz IF signal, for which the following module, AFREG, was designed. AFREG provides the recovered data and clock signals, which are then used in the digital equipment to be described in a subsequent article.

The demodulation procedure in AFREG occurs in two stages. Initially an auxiliary carrier is generated, with which the received signal is compared, to decide whether a phase of 0 or 180 degrees was sent. Using this auxiliary carrier, a raw (noisy) data stream is obtained in a phase-sensitive demodulator.

In the second stage, the data clock is initially extracted from this raw data stream. Using it the raw data bits are then each determined during a bit period; at the end of each data bit, the median value is used in order to decide whether a 0 or a 1 was "more likely" sent. (This technique is also called integration; it provides the best possible estimated value for the data).

In fact, the demodulation of the data using this scheme is quite simple. Unfortunately, the recovery of the carrier and the data clock is, on the other hand, more complicated, and it may seem surprising that the recovery of the carrier and clock signals in PSK causes the most complication.

The Operation of the Data Demodulator AFREG

The module AFREG is a further development of the equipment used at the command stations for OSCAR-10. The experiences gathered in that area have all been incorporated. All the same, it was possible using several tricks to design the module to be simple and easily reproducible. Its development and design up to the present form took nearly two years; in addition to the three authors, Robin Gape, G8DQX, contributed significantly to it.

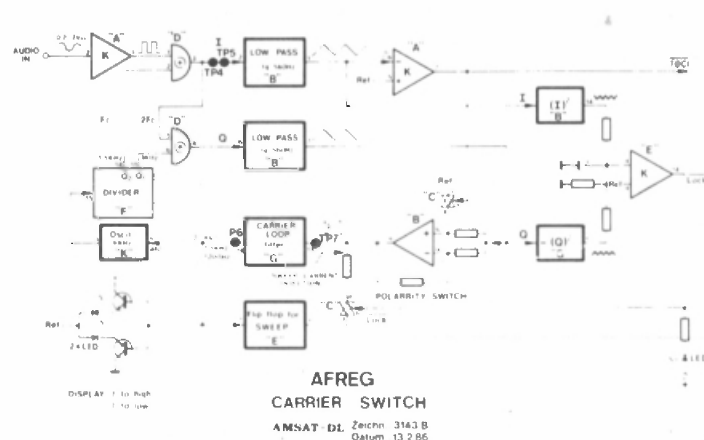


Figure 2 — AFREG carrier switch.

Demodulation

To further understand the circuit, see the block diagram in Figure 2. The audio frequency signal from the SSB receiver is initially limited in a comparator (converted to a square-wave-signal). Therefore the output level from the receiver is no longer very critical (50 mVss to 2 Vss), additionally simplifying the further processing of the signal. The limiting has practically no effect on efficiency in the presence of noise.

The signal coming from the comparator is then compared in an exclusive-OR gate with the likewise square-wave carrier frequency (described later). On these square-wave signals the gate acts as a phase discriminator.

The discriminator output I is passed through a 560 Hz wide lowpass, after which the raw data signal is available.

Carrier Recovery

Where does the carrier come from? The oscillator K, running at approximately 6 KHz, is converted down to 1.5 KHz by divider F. As a rule, this frequency by itself won't be correct. The oscillator frequency is therefore tunable (AFC), and an appropriate circuit has to make sure that the correct frequency is maintained. For this a second discriminator, with the output signal Q, is provided. It receives the same auxiliary carrier as the I discriminator, however with the phase shifted 90 degrees. (In actuality the output of the I discriminator is combined with the double of the carrier frequency. If the corresponding curves are drawn, it is seen that this is equivalent to the above description.)

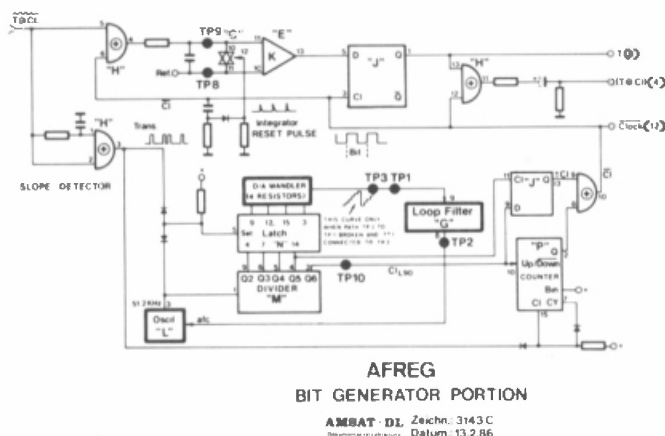


Figure 3 — AFREG bit regenerator.

If carrier frequency and phase are exactly in tune, there is no signal from the Q discriminator. If the phase of the auxiliary carrier drifts away from the ideal value, a signal then exists at the output of the Q discriminator, which is used to pull the oscillator frequency, such that the phase error returns to zero.

Unfortunately the matter isn't quite so simple. The output signal of the Q discriminator could equally be positive or negative for the same phase error, depending on the data being sent. To eliminate this deficiency, the filtered I signal is fed to a comparator, where the

estimated value for the data polarity actuates the "polarity" switch C. By this means the Q signal at the output of this switch is always available in the correct polarity for controlling the oscillator frequency and phase, after subsequently passing through the low pass filter G.

The Sweep Circuit and the Lock Detector

The control loop is designed for the range of 1250 to 1750 Hz. If the frequency error is greater than 50 Hz, the error voltage from Q is so small, that the circuit won't "catch" the carrier frequency by itself; a sweep circuit is therefore necessary.

For this, a voltage is generated with a flip-flop E, which feeds current into the AFC filter. By this means, its output voltage drifts initially in one direction up to the limit of the sweep range. Then the flip-flop again toggles at the other limit. If the circuit is synchronized with the incoming signal, the sweep current into the AFC filter is blocked by means of the lock signal.

The lock signal is generated by making use of the fact that a large data amplitude is available at the output of the I discriminator, while the Q discriminator provides only a very small error signal when in lock. On the other hand, when the input signal is not synchronized, equal amplitudes come from both the I and Q discriminators.

To obtain the lock signal, the values of I and Q are first approximately squared by a rectifier circuit. These two voltages are compared to each other in the operational amplifier E after passing through low-pass filters. When I is significantly higher than Q, the frequency is synchronized to the incoming signal.

To simplify the operation, the AFC voltage is displayed on a meter and after the carrier is synchronized, the lock lamp lights.

Recovery of the Data Stream

The raw data stream from the I low-pass filter is limited in the previously mentioned comparator, which has practically no effect on the signal quality. Since the data signal is combined with the clock at the transmitter, the procedure must be reversed during demodulation. For this an exclusive-OR gate is again used, which gets the clock on its second input. The resulting raw bits are determined during a bit period, in that the capacitor at TP9 is positively or negatively charged, corresponding to the bit polarity. At the end of the bit period, this charge is checked by a comparator; the result decides whether a 0 or 1 bit is present.

Subsequently the capacitor is momentarily shorted out and the procedure is repeated for the next bit period. The bits are temporarily stored in flip-flop, to have a clean output signal for subsequent processing. Additionally they are exclusive-OR combined with the clock, since some equipment used for the subsequent processing needs this type of signal.

Recovery of the Data Clock

As with the recovery of the carrier, the recovery of the bit clock requires some effort. The limited raw data

bits are initially used to create pulses at each signal edge (i.e., the jump between 0 and 1 or vice versa). These pulses are then used to control oscillator L such that, in a manner similar to the carrier recovery, the clock in the AFREG is phase synchronized with the transmitted clock. In the incoming raw data there is always a signal edge available in the approximate middle of the bit (approximate only due to the noise). At the beginning of the bit period, edges are also found, however not so frequently (only when the bit does not change).

Because the edges are not always present, a more complicated discriminator is required. For this purpose, oscillator L, running at approximately 50 KHz, is divided down to the 400 Hz data rate by divider M. The divider with its outputs can therefore be regarded as a type of counting circuit, which counts from zero to the highest value during a bit period. If a pulse in the meantime comes along and transfers the momentary counter value to a storage register (latch), this counter value gives the time since the last clock edge, i.e., the phase between pulse and clock.

Since the pulse can come just as well in the middle of the bit as well as at the beginning, the comparison can only be performed in such a discriminator at twice the clock frequency. The discriminator is very simple: the four bits of the latched counter are converted by a D/A converter (a grandiose name for four resistors) into an analog error signal, which provides the frequency correction, after appropriate low pass filtering. A sweep circuit is not necessary since the tuning range is very small. The only peculiarity is an interlock at the input to the latch to prevent the transfer of the counter values while it continues to count.

Ambiguity of the Clock Phase

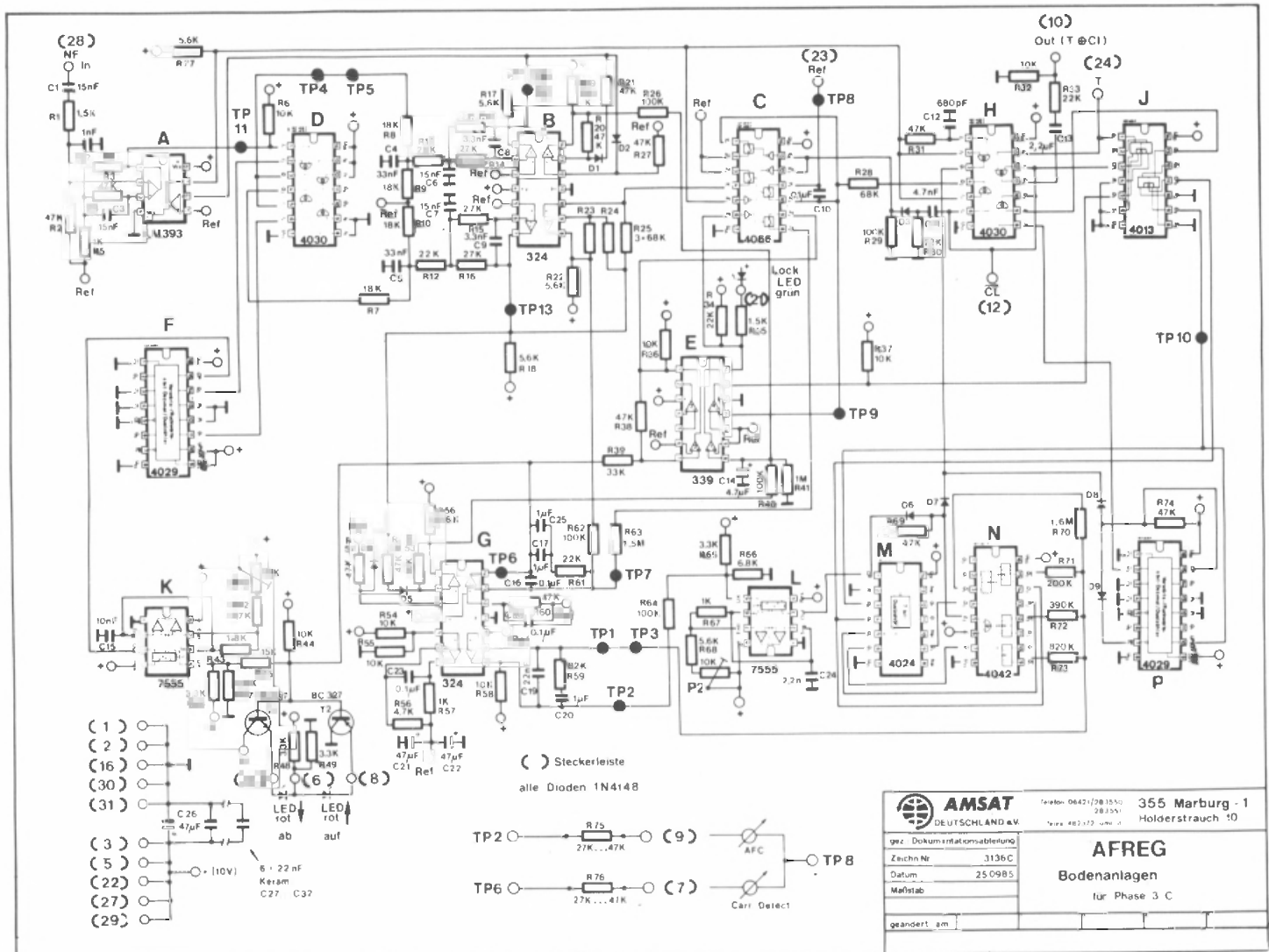
Since the clock recovery occurs at twice the frequency, a further divider stage is necessary to generate the clock itself. Unfortunately, this has an ambiguity of 180 degrees, due to the divider. To eliminate this ambiguity, the edge pulses are used in IC P for the up and down counting so that, in the middle of the bit, the counting is in one direction and, at the beginning of the bit, in the other direction. When the counter reaches its highest, respectively, lowest value, a further counting is prevented by a corresponding interlock.

This circuit causes the counter to stop, according to the clock polarity present, in the vicinity of its highest or lowest values, because the edges are more frequent in the middle of a bit than at the limits of a bit. The most significant bit of the counter provides information about the clock polarity. With an exclusive-OR gate the initially ambiguous clock (+/- C1) is converted to the unambiguous clock C1.

Construction of the AFREG

The AFREG module is installed on a Europe-Card (100mm x 160mm). The other illustrations show the routing of the printed circuit and the positions of the

components. An article on alignment of the AFREG appears elsewhere in this issue. If the demand is sufficient, circuit boards for the AFREG will be made available. Please write the editor to indicate your interest.



Alignment of the AFREG Board

by
Heinz Moelleken, DL3AH

(Reprinted from *AMSAT-DL Journal*, Vol. 13, No. 3)

(Translated by Don Moe, DJ0HC/KE6MN)

Abstract

The function of the satellite telemetry interface was thoroughly described in a previous article. In this part we come to the practical portion: alignment. Since then a few additional changes were made in the circuit and component numbers were assigned, so this is hopefully the final version.

Required Test Equipment

For the alignment of the AFREG board, the following test equipment and materials are necessary:

- Completed AFREG board with all components installed
- 1 $\mu\text{F}/35\text{V}$ MKT capacitor
- Oscilloscope and pick-up lead
- Audio generator (sine/square-wave, preferably with a digital counter for accuracy)
- Power supply +10 V (approx. 500 mA)

Preliminary Steps

Apply the supply voltage ($U_B = +10\text{ V}$) and ground to the board, and measure a current drain of approximately 20 to 40 mA, with jumpers installed between TP4/TP5 and TP1/TP3. (+ U_B to connector pins 3, 5, 22, 27 or 29; ground to pins 1, 2, 16, 30 or 31.) If the current drain is significantly higher or lower, check the board for opens, shorts or incorrectly installed components and correct the problem(s). The three LED's (Lock = green, up/down = red) should be connected to the connector pins according to the schematic.

Alignment of the AF-Demodulator Portion

Feed a sine-wave signal of 1500 Hz at 2 V into the input of the circuit on pin 28. Using the oscilloscope check test point TP11 for a square-wave signal with an amplitude of 10 V. Then reduce the input signal to the level at which the square-wave picture becomes unstable.

As a comparison, with an input voltage of typically 0.2 V ($f = 1500\text{ Hz}$), the square-wave signal should be present at TP11. Increase the input signal level to 2 V again.

Measurement of the Reference Voltage

The reference voltage at TP8 should be +5 V. To generate the reference voltage, IC G is used along with the components on pins 5, 6 and 7.

Short together TP6 and TP7. Connect the oscilloscope to TP12. A triangular-wave voltage of 4 V should be seen (Figure 1). By adjusting the trimmer pot P1 (right-hand pot below IC K), the frequency of the triangular-wave signal is reduced to zero. (The period is adjusted to be virtually infinitely large.) The wiper of the pot should not be at its stop following adjustment.

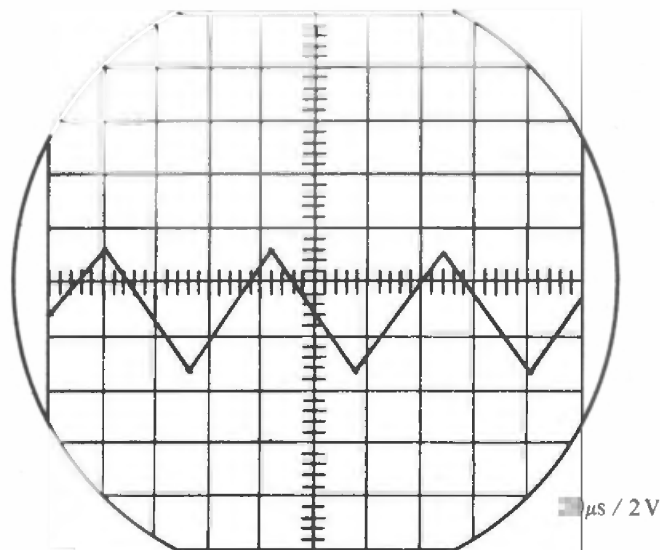


Figure 1—Triangular-wave voltage of 4 Volts at TP12.

Check Measurement

An identical signal should appear on the oscilloscope on TP13 as in the previous alignment. On IC K pin 3 (or IC F pin 15) there should be a square-wave voltage of approximately 12 KHz. (Appearance: negative pulse with a keying ratio of around 10% on and 80% off, Figure 2.)

Raise the input frequency at the audio input (connector pin 28) to $f = 2060\text{ Hz}$, at 2 V. The level of the output voltage at TP12 and TP13 should not be below 3 V (frequency approx. 560 Hz). This measurement serves as confirmation and as a check of the filter at IC B.

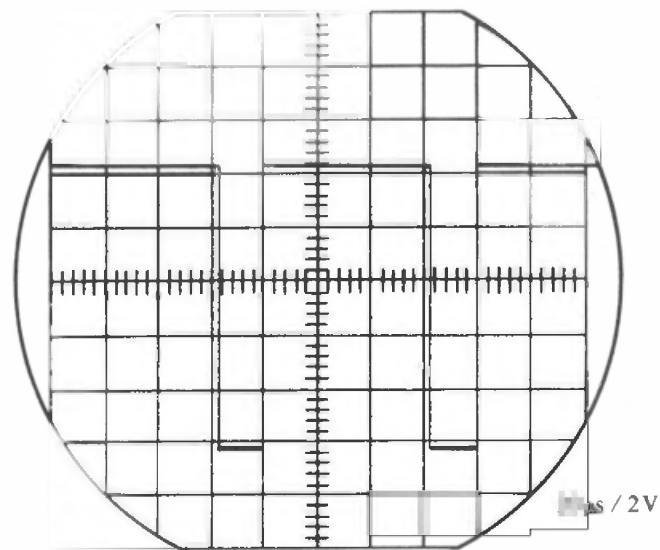


Figure 2—Square-wave of about 12 KHz. at IC-K pin 3.

Set the input frequency to $f = 1800$ Hz (sine-wave) at 2 V. Measured with the oscilloscope, pin 14 of IC B should be +1.5 V and pin 1 of IC G should be -1.5 V, compared with the reference voltage UREF. Open the bridge between TP6 and TP7. Set the input signal to $f = 1500$ Hz and 2 V. The "Lock LED" (cathode to connector pin 21, anode to +UB) must light up.

Remove the input signal from connector pin 28, so that the audio input is open. Check the voltage on TP6 with the oscilloscope. With open input, it should cycle between +2V and +8V at around a 10 second rate. During a cycle, the red LEDs "Up" and "Down" (on connector pins 4, 6, 8) should light up once each per cycle. Depending on the type of LED used, the brightness may vary. This can be adjusted by changing resistors R48 and R49, keeping the current in each diode to maximum 10-20 mA. Feed the sine-wave signal ($f = 1500$ Hz, 2V) into the audio input again (connector pin 28). The "Lock LED" should light and there should be +5V on TP6.

The following measurements serve to check the tuning range of the carrier oscillator. Raise the input frequency until +2V is on TP6. The frequency should then be $f = 1650$ Hz. Lower the frequency until +8V is on TP6. The input frequency should then be $f = 1350$ Hz. Using the oscilloscope, measure the comparison voltage between the reference voltage and IC E pin 8:

- in lock ($f = 1500$ Hz in input): voltage = +0.6V compared to UREF.
- out of lock (no input signal): voltage = -0.2V compared to UREF.

If all of the above values are obtained, the alignment of the lock detector is completed. The AF-Demodulator portion of the board should work perfectly.

Alignment of the Bit Regenerator

Open the bridge between TP4 and TP5. Feed in an audio square-wave signal ($f = 400$ Hz, 4 V) to TP5 using a 1 uF/35V MKT capacitor (not an electrolytic).

Check

On TP12 is a sine-wave signal of 2 V. On IC A pin 7 is a square-wave signal of 10 V, where the positive edge looks a bit ragged. On IC H pin 3 there are positive pulses at 800 Hz with a pulse duration of 20 to 30 us. The pulses have some jitter and each pulse varies slightly.

Connect TP1 with TP2 and remove the solder jumper between TP1 and TP3. The oscilloscope should show a saw-tooth shaped staircase voltage on TP3 (Figure 3). Using the trimmer pot P2 (next to TP2), adjust it so that the period length of the voltage on TP3 is as large as possible (touchy adjustment).

Check

Frequency on IC L pin 3 is approximately 51.2 KHz. Frequency on IC M pin 3 is approximately 400 Hz.

Again open the bridge between TP1 and TP2, and reconnect TP1 with TP3. The reference voltage on TP2 should have very low ripple content.

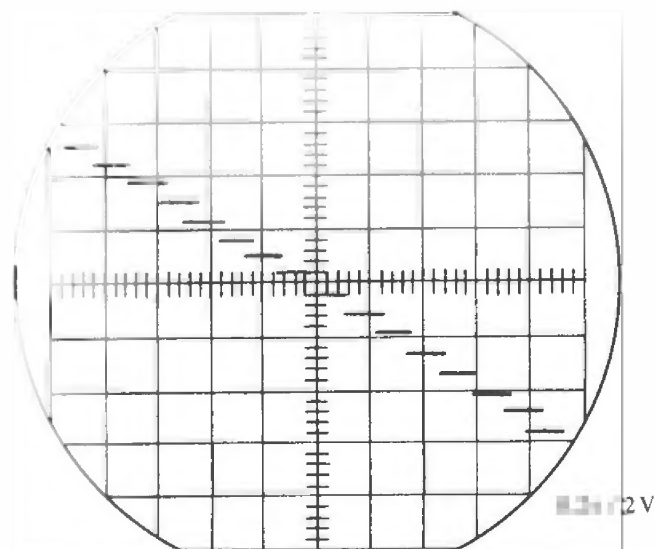


Figure 3—Saw-tooth shaped staircase voltage at TP3.

Now check the tuning range of the oscillator. Change the 400 Hz input frequency by ± 8 Hz. With an input frequency of 408 Hz, the voltage on TP2 is approximately +2 V. With an input frequency of 392 Hz, the voltage on TP2 is approximately +8 V. If these values are obtained, the tuning range of the oscillator (PLL range) is correct, with a 2% tolerance.

Set the input frequency on TP5 to $f = 200$ Hz, square-wave, 4 V. On TP9, the oscilloscope should show a wave form with short rising and falling integration slopes (figure 4). This means that integration occurs for one bit period. Repeatedly disconnect and reconnect the input voltage at TP5 ($f = 200$ Hz), ten times. The wave form for upwards and downwards integration should stay the same, as seen on the oscilloscope.

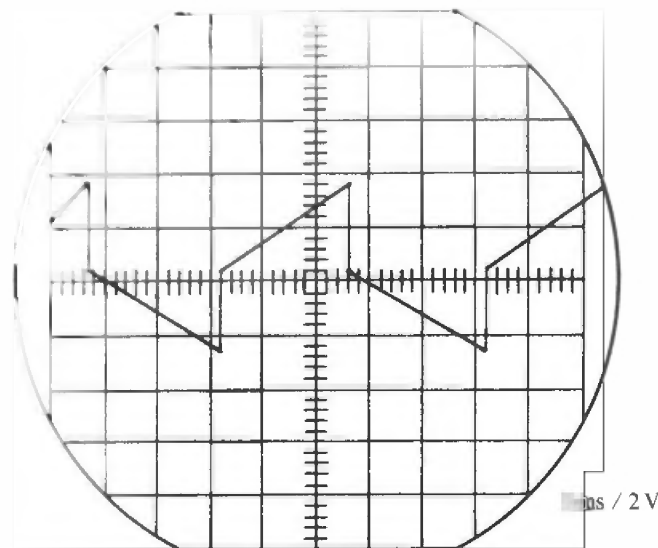


Figure 4—Waveform with short rising and falling integration slopes at TP9.

Simulate a fault by grounding IC P pin 15. This results in a rippling triangular wave shape, different from the previous wave form, when the input voltage is repeatedly connected. However, occasionally the correct wave form may appear briefly. Thereby we see that the polarity recognition isn't working. The simulated fault is eliminated by removing ground from IC P pin 15. Normal operation should be restored.

Tracing the Signal Path to the Output

Check

At the output of comparator IC E, pin 13, there is the 200 Hz square-wave signal at 10 V. A square-wave voltage of 3 V with no DC component is on the output connector pin 10.

The input frequency on TP5 (via 1 μ F capacitor) is raised to 400 Hz. If everything was OK thus far, the frequency at the output must also be 400 Hz. This completes the alignment of the bit regenerator portion. Close the bridge between TP4 and TP5 again and remove the capacitor from TP5.

Component List for AFREG-01

1. Resistors (RM10, 5%, 1/4W)

R5, R57, R67 1 k Ω m
 R1, R35 1.5 k Ω m
 R43 1.8 k Ω m
 R46, R48, R49, R65 3.3 k Ω m
 R42, R56 4.7 k Ω m
 R17, R18, R19, R22, R50, R68, R77 5.6 k Ω m
 R47, R66 6.8 k Ω m
 R6, R32, R36, R37, R44, R54, R55, R58 10 k Ω m
 R45 15 k Ω m
 R7, R8, R9, R10 18 k Ω m
 R11, R12, R30, R33, R34, R61 22 k Ω m
 R13, R14, R15, R16 27 k Ω m
 R39 33 k Ω m
 R2, R4, R20, R21, R27, R31, R38, R51, R52, R53, R60, R69, R74 47 k Ω m
 R23, R24, R25, R28 68 k Ω m
 R59 82 k Ω m
 R26, R29, R40, R62, R64 100 k Ω m
 R71 200 k Ω m
 R72 390 k Ω m
 R73 820 k Ω m
 R3, R41 1 M Ω m
 R63 1.5 M Ω m
 R70 1.6 M Ω m
 R75, R76 (depending on meter)
 27 to 47 k Ω m

2. Capacitors

(RM-5, RM-7.5, min.20V, MKT)

C2 1 nF
 C24 2.2 nF
 C8, C9 3.3 nF
 C11 4.7 nF
 C15 10 nF
 C1, C3, C6, C7 15 nF
 C19 22 nF

C27, C28, C29, C30, C31, C32 (Disc-ceramic, RM-2.5/5) 22 nF

C4, C5 33 nF

C12, 680 pF

C10, C16, C18, C23 0.1 μ F

C17, C20, C25 1 μ F

C13 (RM-10/12, 5/15) 2.2 μ F

C14 (Tantalum) 4.7 μ F

C21, C22, C26 (Electrolytic) 47 μ F

3. Diodes

D1, D2, D3, D4, D5, D6, D7, D8, D9 1N-4148

4. Integrated Circuits

IC J CD-4013

IC M CD-4024

IC F, IC P CD-4029

IC D, IC H CD-4030

IC N CD-4042

IC C CD-4066

IC K, IC L ICM-7555

IC B, IC G LM-324

IC E LM-339

IC A LM-393

5. Transistors

T1 BC-337

T2 BC-327

6. Potentiometer

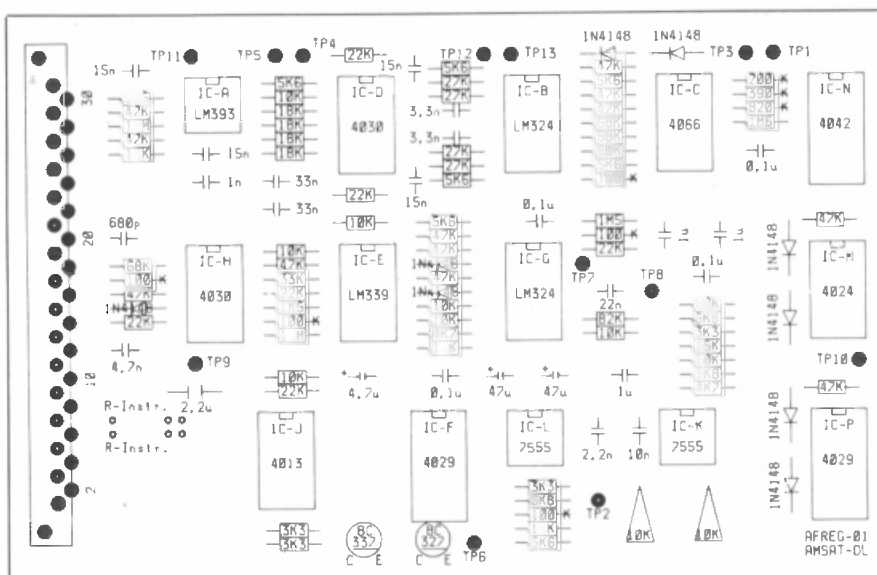
P1, P2 (RM-5, horizontal) 10 k Ω m

7. Parts needed for alignment

2 LED Red

1 LED Green

1 Capacitor, 1 μ F, MKT.



A Proposed Series of Satellites for Digital Message Relay

by

Gerry Creager, N5JXS

2601 S. Braeswood No. 801, Houston, Texas 77025

ABSTRACT

Explosive growth in Amateur Radio's use of digital communications has occurred since the implementation of AX.25, an adaptation of the CCITT X.25 switched packet network protocol. We propose to promote interest in the Amateur Radio satellite program by implementing a series of orbiting satellites dedicated to digital communications. Central to our concept are the following: to maximize the user base by designing the system for use by a prototypical Mode B station; and minimize the amount of modification expected on otherwise usable Packet radio equipment by adhering to the existing AX.25 protocol implementations regarding data encoding, data rates and modem access.

A minimum of two satellites is planned. The first phase of the experiment proposes launch of a "concept" implementation of the final system hardware and software from a Shuttle (STS) Getaway Special into a low-earth orbit, with final orbital insertion accomplished us-

ing a thermal-expansion (Freon 114) based perigee kick motor. The second phase of the experiment proposes one or more satellites in a higher orbit, with the advantages of longer window, more access area and less doppler shift.

Both phases will share some commonality: an orbiting digital packet repeater, a single channel device, with input and output on the chosen satellite beacon frequency; and a store-and-forward messaging system. The digital hardware will be designed by the Houston group. Spaceframe design and fabrication will be undertaken by the Phase III-C group in Boulder, CO. Radio frequency components will be designed and fabricated by the Motorola Amateur Radio Club in Plantation, Florida. Thermal design and control will be overseen by Richard Jansson, of Phase 3 fame. Design and implementation of the Packet Technology Satellite Experiment is expected to require at least three years.

Introduction

Packet Radio (Packet) has enjoyed a marked enthusiasm since it was introduced several years ago. Packet arose as an outgrowth of the computer communications revolution. An adaptation of the CCITT X.25 switched packet network protocol, known in the Packet world as AX.25, allowed incorporation of entire Amateur Radio callsigns as well as intermediate relay path information (digital repeaters or "digipeaters") in the address field. The Tuscon Amateur Packet Radio Corporation (TAPR) designed the first commercially available terminal node controllers (TNC). Several manufacturers offered equipment including licensed TAPR designs, and other hardware designed to implement terminal node controller functionality. A comprehensive redesign effort by TAPR resulted in enhanced operation in the form of the TNC-2. Recent additions to the state of the art include IBM-PC plug-in TNC's; controllers specifically for the Apple MacIntosh, hardware-software combinations for the Commodore

64 and 128, and specialty devices which allow use of several of the digital modes including Packet, AMTOR (Amateur Teleprinting Over Radio), RTTY (radio teletype), and Morse code. One manufacturer estimates over 15,000 TNC's have been sold to date to the Amateur community.

Several groups have proposed and implemented digital communications experiments for orbiting Amateur satellites. These include the digital communications experiment on UoSAT-2 (OSCAR-11), the Phase III-B (OSCAR-10) message system, the RUDAK store and forward system for Phase III-C and the digital transponder and messaging system on JAS-1 (Fuji OSCAR-12). The Houston-based Packet Technology Satellite Experiment (PTSE) proposes a series of orbiting satellites designed for Amateur Packet communications. The considerations which led to this proposal are discussed below.

Of primary concern in the design of the PTSE is maximization of the user base and minimization of modifica-

tions to standard Packet hardware. Therefore, we have decided that a narrow-band frequency modulated signal, utilizing audio frequency shift keying (AFSK) would be employed for both uplink and downlink. Standard TNC modem tones (based on the Bell 202 standard) will be used so that the TNC may be used for non-satellite applications as well. Use of standard modem tones will allow current Packet users to utilize the orbital system without having to significantly modify their existing equipment. The system is being designed to serve the typical Mode B station for Phase 1 implementation (100 watts effective isotropic radiated power [EIRP], 14 decibels isotropic reference [dBi] transmitter antenna gain). This should invite current satellite users to utilize the PTSE without suffering significant financial penalty. Additionally, the Amateur who has not been active on the satellites can acquire the equipment necessary to access the system without bankrupting the family budget.

Two hardware objectives are being considered in development of the Packet Technology Satellite Experiment. These are a digipeater, and a store-and-forward message system. Both of these types of subsystems have been adequately proven in terrestrial applications. The orbiting digipeater will function similarly to a terrestrial digipeater—if a station chooses to include the orbiting digipeater in its connect or unprotocol communications path, the digipeater will receive and subsequently retransmit the digital signal on the same frequency that received it. In addition, the digipeater output will serve as a beacon, transmitting information related to spacecraft status and conditions.

The store-and-forward, or messaging, system will perform a function similar to a terrestrial Packet Bulletin Board System (PBBS). The user will have the option of sending a message, reading one left for him or killing any messages where he was either the sender or addressee. The messaging system will allow run-string input of information, or else will prompt the user for required information. Messages will be constrained to one 80 by 25 screen of data, or approximately 2000 bytes. By design, messages must be preconceived, composed using a text editor or word processor, and then uploaded to the satellite. 'Hunt and peck' input will only result in incomplete (and therefore, non-stored) messages. This is intended to reduce the time a station is necessarily connected to the satellite, a serious consideration in a low earth orbit with relatively short windows of access.

Complete hardware specifications are currently being developed. Current specifications under investigation include the use of complementary metal oxide-silicon (CMOS) technology for all integrated circuits to reduce power requirements, static random access memory (RAM) to eliminate the requirement for periodic memory refresh, a large, addressable memory space to accommodate store-and-forward user messages, and error detection and correction hardware and algorithms to detect and correct single bit errors and simply detect and flag multiple, sequential bit errors. A large array of memory, properly managed, allows

logical removal of a block of memory in the event of hard failure.

Software specifications are also under development, pending finalization of the hardware design. Software requirements include the user interface, store-and-forward functionality, spacecraft housekeeping functions and digipeater operations. In brief, the spacecraft software will provide a user interface that is simple and straightforward, but not necessarily 'user friendly', to access the messaging system. Commands common to the WORLI system will be incorporated, if feasible, to allow the user a comfortable mode of operation. However, the satellite is NOT a bulletin board; it merely provides one of the functions thereof.

Method of Implementation

The Packet Technology Satellite Experiment will proceed in two phases. The first phase will include initial design of all spacecraft hardware and software, initial fabrication of subsystems and deployment of a prototype in low-earth orbit to prove the concepts proposed in this experiment. The Phase one spacecraft will essentially be a prototype and proving ground for the Phase two series. Phase 1 is currently envisioned to include a co-channel (shared uplink and downlink) digipeater and two messaging system channels operating in AMSAT Mode B (70 cm uplink, 2 meter downlink) with a single downlink channel shared between the two uplink channels.

Onboard computer coordination of the messaging system downlink channel is planned to improve channel utilization. Process specific CMOS (complementary metal oxide-silicon) microprocessors will be employed for coordination of individual tasks. Implementation of multiple processors, incorporated with a central databus, allows the processor best suited for a task to initially perform that task, but allows redirection of any processor to any task in the event of failure of a subsystem.

The radio-frequency (RF) components for Phase 1 are to be designed and implemented from standard Motorola Communications modular subsystems to address specific design criteria and specifications. We are anticipating direct current to RF efficiencies of approximately 30-45% for the transmitters when matched to appropriate antennas on the spacecraft. Current transmitter design specifications include a channelized frequency synthesizer design capable of up to 6 watts output. The receivers should be sufficiently broad-band to allow tracking and capture of doppler induced uplink frequency errors, automatic frequency control to track off frequency signals in the center of the passband, sufficiently low noise figures to allow input preamplification without degradation of performance due to a poor signal to noise ratio, and frequency agility to allow command stations the ability move the receivers in the event of natural or man-made interference.

Testing of the Phase 2 spacecraft designs will begin with the Phase 1 deployment. In Phase 2, the basic craft is planned to include a 145 MHz digipeater and a number of Mode B-type (435 MHz uplink, 145 MHz downlink)

or Mode L-type (1.2 GHz uplink, 435 MHz downlink) store and forward channels. The messaging system channels will be segregated by functionality. Two uplink channels will be dedicated to storage of messages for each three uplink channels dedicated to message retrieval. At least two downlink channels will be used. Both will be controlled by the onboard computer to promote better channel utilization; one will be dedicated to message uploading, and one to retrieval. The digipeater transmitter channel will function as the spacecraft telemetry beacon. Current spacecraft status will be routinely transmitted, channel loading permitting. The spacecraft housekeeping processor will accumulate periodic data and store it in a file for retrieval by interested stations by connecting to a telemetry address. The use of AX.25 to format and transmit the telemetry data allows a command station to automate satellite monitoring to a degree not previously realized. We anticipate developing software to promote distributed command stations transmitting telemetry back to Houston for archiving and analysis. Phase 1 will incorporate a model of the Phase 2 computer system. Program code in Phase 1 will be similar to that currently planned for Phase 2, but modified to accommodate the fact that only two store-and-forward channels will fly on it. The digipeater is common to both spacecraft.

The orbit proposed for Phase 1 is approximately 800 kilometers (500 statute miles), circular. We propose to utilize the Freon-114 perigee kick technology developed by Rick Fleeter for UoSAT/PACSAT to propel the PTSE satellite from a 300 km Space Transportation System (STS) Shuttle orbit to 800 km. To date, no Shuttle Getaway Special has been approved for launch with any type of propulsion system in place. A stable circular orbit of this altitude will have a period of approximately 95 minutes and an overhead pass acquisition window of over 10 minutes. The orbits being discussed for the second phase of the project will require a different propulsion system because of the increased mass, and the higher velocity vector required to place an object in a higher orbit. NASA is currently investigating the possibility of a low-cost, Shuttle launched package, in the "Scout-class" range capable of lifting a 200-400 kilogram (kg) payload to geosynchronous orbit. It is our considered opinion that the benefits of a high orbit realized in long acquisition window, ease of tracking and small doppler shift will adequately counter the problems of deployment and increased used power considerations.

Project Support Personnel and Timetable

Several groups have expressed an interest in working with the Houston group, or have been actively solicited. The Motorola Amateur Radio Club, Plantation, Florida, who provided the communications equipment for

W5LFL and W0ORE during their "Ham in Space" and SAREX (Shuttle Amateur Radio Experiment) missions have expressed an interest in designing and qualifying the spacecraft RF components. Jan King and the Phase III-C group from Boulder, Colorado, have been recruited to provide their expertise in spaceframe design and power bus design to our effort. Rick Fleeter, designer of the PACSAT propulsion system, has been approached to act as propulsion engineer and consultant for the PTSE. Richard Jansson, thermal designer for the AMSAT Phase 3 effort has agreed to act in a similar capacity for our effort. Local involvement has provided expertise in orbital mechanics, guidance, navigation and control, computer hardware systems, software systems, user interface, analog systems (telemetry), printed circuit design and fabrication, integrated circuits quality assurance and control, Shuttle payload integration and solar power systems. In general, an outpouring of support has indicated that all pertinent areas for design consideration have been addressed either within the Houston group or by outside expertise.

We anticipate that a minimum of three years will be required to bring the first phase of the project to a conclusion. Much of the reason for the extended time line is due to the grounding of the Shuttle fleet following the Challenger accident. Additionally, the need to develop new computer designs specifically for this project and to thoroughly qualify new hardware and software, will prove time intensive. Component selection, subsystem assembly and troubleshooting, and extensive ground testing will also impose large time requirements. The current short term goal, nonetheless, is to complete a prototype hardware system within six months to allow software implementation and realtime testing of the hardware and software.

Conclusion

We are undertaking the design, development, fabrication, and deployment of a series of satellites designed for digital communications relay. Specific design criteria include planning for use by a standard OSCAR earth-station and utilization of current AX.25 technology (to preclude the modification of otherwise useful packet equipment). The spacecraft will provide message forwarding functions as well as a digipeater to relay Packet radio signals. The first phase of our project proposes deployment of a prototype of the second phase spacecraft into an 800 km circular orbit to provide an early implementation of the satellite for general use and to provide a test bed for continuing Phase 2 development. We anticipate the project will require significant effort for at least three years through completion.

Power Budget and Eclipse Considerations for PTSE-H

by Courtney Duncan, N5BF
14131 Prestonwood Forest Drive
Houston, TX 77070

ABSTRACT

Power requirements and power availability for a phase I PTSE-H mission are studied. Estimates of subsystem consumption for various operational and user loading cases are considered. Estimates are made of power available for the satellite configuration and orbit considering eclipsing, orientation, and stabilization. An orbit of 800 Km altitude and 57 degrees inclination is considered primarily, other orbits are discussed for comparison. Comparisons are made between required and available power and mission management guidelines are suggested. Further study and refinement of estimates employed in this study is recommended.

Introduction and Purpose

Most earth orbiting satellites are powered by solar cells and batteries in combination. The solar cells collect energy from solar radiation which is used to directly power satellite electronics and charge storage batteries. During eclipse periods (when the satellite is in darkness) the battery provides all of the electricity to the satellite.

The purpose of this report is to analyze, to first order, the power budget for the Packet Technology Satellite Experiment-Houston (PTSE-H), also known as HouSat. Emphasis is placed on the targeted orbits and the eclipsing properties of those orbits. Eclipsing analysis will also prove helpful in analyzing the thermal requirements of the satellite.

This is a first order study. Many estimates are completely unfounded and most calculations are made for only simple "best" and "worst" cases. The goal is to provide a point for data collection and analysis in order that power constraints and realities are well understood. As data is obtained from prototyping or from more detailed analysis, conclusions and project planning will be refined accordingly.

Study Outline

The power budget is considered from two points of view. Power required to meet mission objectives as a function of time and loading is compared with power and energy storage available.

This study is organized into four parts:

- 1) statement of mission objectives,
- 2) estimate of power required to meet mission objectives,
- 3) estimate of power available in a possible trajectory,
- 4) comparisons between power required and power available, and
- 5) conclusions and recommendations for refinement of the study.

Mission Objectives

The PTSE-H mission goal is to provide an orbiting digital mailbox with continuous service. An experimental digipeater will also be included. Ideally, all computer functions would be kept powered at all times, all library memory, the transmitter, and receivers would always be available to users. As this will not be practical under all circumstances of user loading, eclipsing, and component life, system design allows for dynamic and semi automatic allocation of resources to maintain the health of the spacecraft power system.

Eight megabytes of memory are envisioned for the library processor where messages will be organized and stored. This memory will be arranged so that only the part which is actually storing messages at a given time will be powered. If required, a maximum storage limit can be set so that not all memory is available.

Spacecraft processors may be put into sleep mode so as to minimize their power consumption when not in use. The transmitters and user receivers may be turned off periodically (one or more days a week) for power system recovery but the mission concept requires that some part of the library memory be kept powered at all times. Otherwise a dependable, long term, data storage and retrieval system is not realized.

With transmitter power fixed and spacecraft overhead power requirements minimized, energy will be conserved in order to allow library RAM and library CPU time to be made available for user messaging.

Estimate of Power Requirements

Spacecraft power systems are considered in three sections, radio frequency (RF) components, messaging system components, and spacecraft command and overhead components. System loading is considered for five generalized cases, unloaded, fully loaded, overloaded, recharging, and maneuvering. An active digipeater experiment will about double the transmitter power requirement if it is operated simultaneously with the messaging system. This experiment is not considered in the estimates developed below.

In unloaded state, the spacecraft is over an unpopulated part of the world. All receivers are functioning but since there is no user input, the transmitter has a 5% duty cycle or less as it transmits short bulletins and telemetry a few times a minute. The computers are all powered but most are in sleep state.

In fully loaded state, the spacecraft has up to 20 current users, a maximum of five per receive channel. User packets are received at a 50% to 100% success rate. The transmitter is on at least 95% of the time and the computers are generally active.

In overloaded state, enough users are attempting to use the system that packet success is less than 50%. Stronger stations will be able to capture one of the receivers occasionally, so the transmitter will have a 30%-50% duty cycle. The computers are generally active.

While recharging, the satellite is made unavailable to users. A command receiver and perhaps an occasional packet beacon transmission are maintained. All unused CPUs are put to sleep; only memory that contains active messages is powered, and unused receivers are turned off.

Maneuvering mode is like recharge except that the housekeeping computer is active controlling maneuvers. Power will be required by fuel heaters or igniters, magnetotorquers, motors to deploy or retract booms or antennas, and other equipment of this type.

Transmitter and receiver

The proposed transmitter is to put out 4 watts at a 70% DC to RF conversion efficiency. Estimate 1 watt drain with key up.

Table 1 — Transmitter Power Summary

Loading	Duty Cycle	Power
unloaded	5%	1.2 W
full	95%	5.5
overload	40%	2.9
recharge	0%	0.0
maneuver	5%	1.2

The proposed receivers are known to consume 50 mA squelched and up to 200 mA unsquelched at full audio. Since the receivers will not have to supply significant audio power to the PAD hardware, their unsquelched consumption is estimated at 75 mA. These currents are assumed to be taken directly from the 10 volt spacecraft power bus. Duty cycle is the percentage of unsquelched time per receiver.

Table 2—Receiver Power Summary

Loading	Number used	Duty cycle	Power
unloaded	4	1%	2.0 W
full	4	40%	2.4
overload	4	100%	3.0
recharge	1	1%	0.5
maneuver	1	5%	0.5

Onboard Logic

The onboard digital system will be comprised of three subsystems, the messaging library (containing 8 Mbytes of 12 bit RAM and run by an 80C86RH CPU), the PAD board (a 64180 CPU with 512 Kbytes of RAM) and the IHU/telemetry board (6811 CPU). Current estimates give the following five volt current requirements for these boards.

Table 3—Logic Boards Power by Mode

board	functioning	sleeping
IHU/TLM	500 mA	*
PAD	500 mA	1 mA
library	2500 mA	250 mA

** The IHU/telemetry CPU will only be powered down in the case of a board failure. If this occurs, the library computer will assume IHU duties and will be able to collect some of the more critical telemetry parameters.*

The library RAM is expected to consume about 30 mA per Mbyte and any RAM not currently used by messages will be switched off. With low message content, the sleep mode of the library board can occur at very low current but estimates made here are based on full memory usage. Logic activity levels do not influence power requirement estimates to the degree of accuracy now available. Note that the library board can be put to sleep without losing memory contents.

In this table the estimates have been converted to power requirements from the 10 volt bus allowing a generous 40% regulator inefficiency and translating into the five standard activity cases.

Table 4—Logic Power Summary

Loading	Usage	Power
	a = active s = sleep ihu pad lib	
unloaded	a a a	24.5 W
full	a a a	24.5
overload	a a a	24.5
recharge	a s s	5.3
maneuver	a s s	5.3
conserve	a a s	8.8

The library computer is a major item in the spacecraft power budget and the 8086 will also be doing any number intensive calculations such as orbit determination. The PAD computer, with 512 Kbytes of RAM available to it, can offload some of the messaging functions and some of the messages while the library system sleeps to conserve energy. For this case, the satellite usage case "conserve" has been added to reflect power requirements of the logic system when the satellite is fully active and the library computer is asleep but "on call."

With the hardware arrangement proposed and by the nature of packet radio, a list may be kept of satellite users and locations and compared to known satellite positions in order to offload the messages most likely to be requested over a period of time when the library is asleep. Of course, the PAD board will be able to

awaken the library system at any time, provided energy is available, for messaging, local memory shortage, or spacecraft management reasons.

This spacecraft will have a new capability within the amateur satellite service, that is, to directly collect demographic data based on usage and allow the control team to select an operating procedure and spacecraft control algorithms based on that exact data.

Maneuvering and Stabilization Equipment

This mission is unlikely to be deployed into exactly the right orbit, attitude, and stabilization directly from the launcher. A freon based propulsion system, proposed by Fleeter for PACSAT, requires a heater in the jet nozzle. Magnetotorquers use electric current to change the spacecraft attitude by acting on the earth's magnetic field. These systems or others like them may require relays, valves, igniters, or other special purpose equipment that will require electrical power enough times to require power budget consideration.

An estimate of power requirements of such a system is 60 watts maximum, applied over a period of several orbits and at most over 5% of each orbit (18 degrees of specific anomaly).

Once the satellite is in the final orbit, attitude, and

stabilization condition, stabilization is to be passive, requiring very little active operation of any attitude control systems. For this reason, power required is estimated at 3% of power used during active maneuvering.

Activities such as boom or antenna deploy ordinarily happen only once and are not considered in the power budget.

Table 5—Satellite Control Power Summary

Loading	Power
unloaded	0.1 watts
full	0.1
overload	0.1
recharge	0.1
maneuver	3.0

Summary

The major power users of the spacecraft have now been considered. In this table the figures are summarized.

Table 6—System Power Requirements, All Logic Functioning

Loading	Tx	Rx	Logic	Control	Total
unloaded	1.2	2.0	24.5	0.1	27.8 W
full	5.5	2.4	24.5	0.1	32.5
overload	2.9	3.0	24.5	0.1	30.5
recharge	0.0	0.5	5.3	0.1	5.9
maneuver	1.2	0.5	5.3	3.0	10.0

Table 7—System Power Requirements "Conserve" Logic Mode

Loading	Tx	Rx	Logic	Control	Total
unloaded	1.2	2.0	8.8	0.1	12.1 W
full	5.5	2.4	8.8	0.1	16.8
overload	2.9	3.0	8.8	0.1	14.8
recharge	0.0	0.5	5.3	0.1	5.9
maneuver	1.2	0.5	5.3	3.0	10.0

Coverage

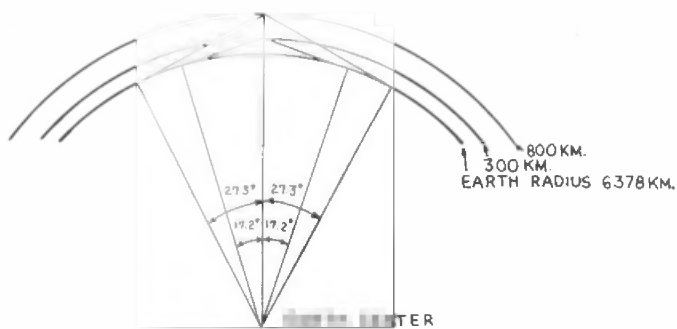
In a separate study it is shown that coverage for users at moderate latitudes is maximized for low earth orbits with inclinations between 40 and 57 degrees. A table from this study is included here for reference. This table

shows the average number of minutes of visibility per day for a user at the indicated latitude for a satellite altitude of 800 Km at various inclinations. Inclinations are given at left, latitudes across the top.

Table 8—Satellite Above Horizon Time per Day, Average

Satellite Altitude 800 Km								
Minimum Elevation 0 degrees								
Minutes/Day at given Latitude								
	Lat	0	15	30	45	60	75	90
Incl								
28	135	127	96	47	0	0	0	
40	86	106	105	80	34	0	0	
57	64	68	90	104	91	53	0	
82	53	55	62	79	130	190	210	
97	53	55	62	79	130	193	212	

The satellite footprint from this altitude has a "radius" of 27.3 degrees of latitude. This corresponds to 28.5 million square kilometers which is 5.6% of the earth's total surface area. A cross section of the earth, satellite, and footprint is shown in Figure 1. The figure is drawn to scale to emphasize the geometry. The problem here is to estimate how much time per day the satellite spends in each of the three user modes, unloaded, loaded, and overloaded.

**Figure 1. Satellite Footprints from 300 km. and 800 km.**

By the nature of the system, it will be overloaded when it is over an area where there is a significant amount of packet radio activity. This includes North America, Europe, Japan, and possibly Australia. Estimate two hours per day over the continents and 95 minutes in view of Japan. Full loading will occur when any other populated area is in view. Light or no loading will occur over unpopulated regions such as the South Pacific. Estimate the remaining time of the day being divided about equally between full and no loading. Assume that the library CPU can sleep during light or no loading periods. This table summarizes the estimated power requirements during the full user access phase of the mission.

Table 9—User Loading Estimate, Minutes per Day

Loading	Minutes/Day	Power, Watts
none	485	12.1
full	500	32.5
over	455	30.5

The average power requirement over a 1440 minute day is 25.0 watts.

The "prime time effect" will influence the daily schedule. Precession of the ascending node will bring the satellite into view at different times of day resulting in different loading patterns. As automated forwarding comes into use in the satellite enhanced packet network, this will tend to smooth out.

This estimate is an educated guess based on satellite operating experience and informal study of a world globe. A unique capability of a packet radio satellite mission is that it will be able to collect demographic data of this sort as part of its routine operation. Such data can then be used to improve current operations and refine planning for future missions.

Finally, power requirements in the three basic modes of operation are summarized.

Table 10—Power Requirements Summary

Operating Mode	Power, Watts	Energy/Day, KJoules
full user access	25.0	2160
recharge	5.9	510
maneuvers	10.0	864

Estimate of Power Available

A model of the energy collection subsystem consists of three parts, the solar cells and batteries, satellite orientation, and eclipsing.

The PACSAT design is an octagonal "cylinder" 24 inches long and with a circumscribed radius of 9.5 inches. This spaceframe is designed to be deployed from

a space shuttle "Getaway Special Cannister." For this first order analysis, this model is used and it is assumed that all of the faces of the octagon (but not the ends of the satellite) are 85% covered with solar cells.

A solar cell can function at full output when it is positioned orthogonal to the incident energy, that is, it is fully illuminated by the sun. To first order, output varies with the cosine of the angle between the normal to the surface incident rays. This model breaks down at high incidence angles because of the refractive properties of the glass coverings. Neglecting this flaw in the model, a cylinder of solar cells can be modeled as a rectangle which is equal in length to the cylinder and as wide as the diameter of the cylinder. The rectangle's orientation in this model is parallel to the cylinder's longitudinal axis and normal to solar incidence.

To modify this model for the octagonal "cylinder," simply realize that the apparent radius changes as the octagon rotates. At minimum, the octagon appears to be of the radius of the inscribed circle, in this case, 8.8 inches. At maximum, the apparent radius is that of the circumscribed circle, 9.5 inches. As the satellite rotates, the apparent radius oscillates between these values. For this analysis, in order to make partial allowance for refraction and other losses, the average apparent radius is taken as the minimum value of 8.8 inches. The model is, therefore, a rectangle 24 inches long, 17.6 inches wide, and 85% covered. This is equivalent to a fully covered area of 359 square inches.

The energy falling on one square centimeter area at normal incidence, outside the earth's atmosphere, at the mean distance of the earth from the sun equals 2.00 small calories per minute. This value varies $\pm 2\%$ (page F-142, 48th CRC handbook) and is equivalent to 0.900 watts per square inch.

The solar panel model is exposed to 323 watts when fully illuminated normal to the sun's rays.

If the longitudinal (or spin) axis is not normal to the sun's rays, this figure decreases with the cosine of the angle of incidence. There is wide orientational leeway since the half power point (162 watts) is at 60 degrees incidence. Figure 2 demonstrates the angle of incidence.

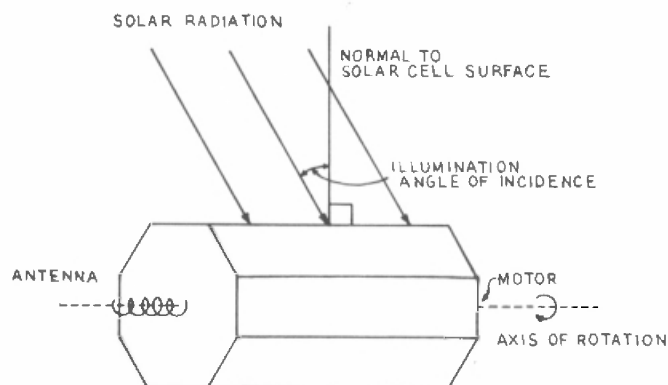


Figure 2. Solar Illumination

Energy collection, antenna pattern, and thermal design all compete for priority in selection of an orientation and stabilization plan.

PTSE-H team member Carl Kotilla, WDSJRD, is developing a detailed analysis of energy conversion, storage, and retrieval efficiency from data in this study. (See the July 1973 *QST* page 67 for an example of how this was done for OSCAR 6.) At this point, assume cell efficiency of 9% and battery charge/discharge efficiency of 80%. This implies a total of 29.0 watts available under best case illumination. Between 64% and 100% of collected energy will be usable depending on how much is used immediately and how much is cycled through battery charge/discharge. Average best case power available could be as low as 18.6 watts at the beginning of the mission when everything is functioning perfectly. For the remainder of this study, inefficiencies in the power collection system are neglected and it is assumed that all available energy can be applied.

The PTSE-H satellite may feature intelligent charge-discharge control if it is deemed advantageous.

As the satellite and the solar cells age over a period of years, degradation in output of 50% to 75% or more can be expected. Batteries deteriorate as well. If the power budget is tight at the beginning of the mission, messaging or accessibility will certainly have to be cut back later.

Satellite Orientation and Eclipsing

Satellite orientation and eclipsing are developed together because their effects on total power available interact. If energy collection is the priority in selecting satellite attitude and stabilization, an attempt will be made to inertially stabilize in one axis and keep the longitudinal axis less than 30 degrees from normal to solar radiation at all times. In this case, the flow of energy from the power system is steady and is interrupted only by eclipsing. This approach will also simplify thermal stability analysis.

If another subsystem, such as the need for "facet down" antenna aiming, is given priority then two axis geocentric stabilization is required and energy collection capability will vary widely, depending on the current ephemeris.

The two stabilization methods are shown in Figures 3 and 4.

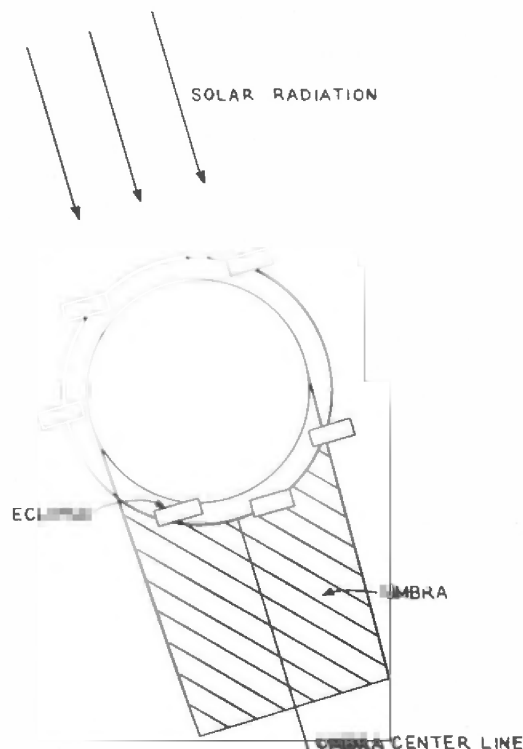


Figure 3. Inertial Stabilization
Not to Scale

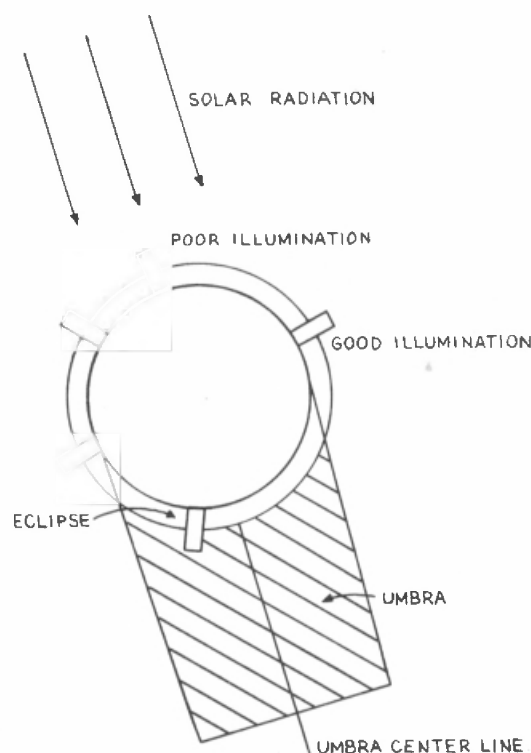


Figure 4. Geocentric Stabilization
Not to Scale

First consider eclipsing percentage and the factors that influence it.

Satellite eclipsing occurs when the spacecraft passes into the earth's shadow. During periods within the shadow, no solar exposure is available for satellite powering. This, too, is a thermal concern.

To first order, the earth's shadow can be modeled as a cone extending away from the earth in a direction exactly opposite to the sun. See Figure 5.

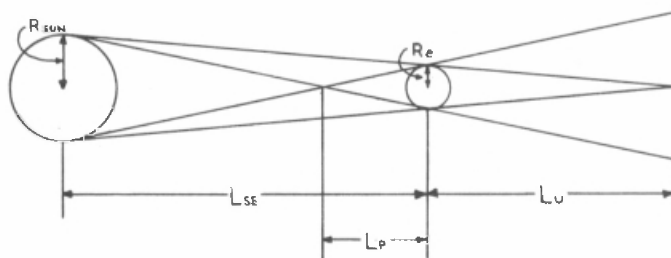


Figure 5. Eclipse Model
Not to Scale

$$\begin{aligned} R_e &= 6,378 \text{ radius of earth} \\ R_{sun} &= 695,300 \text{ radius of sun} \\ L_{se} &= 150,000,000 \text{ distance from center of} \\ &\quad \text{sun to center of earth} \\ L_u &= ? \text{ distance from center of} \\ &\quad \text{earth to apex of umbra} \end{aligned}$$

By similar triangles,

$$L_u/R_e = (L_{se} + L_u)/R_{sun}. \quad (1)$$

This reduces to

$$L_u = L_{se}/((R_{sun}/R_e)-1) \quad (2)$$

and evaluates to

$$L_u = 1,385,000. \quad (3)$$

Beyond this distance from the earth, an object cannot be totally obscured from the sun. Note that this is greater than the distance to the moon (384,000 Km) allowing lunar eclipses.

Incidentally, this same equation evaluates to 376,000 Km for the moon's umbra, thus allowing total "solar" eclipses (by the moon) at the earth's surface (6300 Km closer) only when the moon is slightly closer than its average distance from the earth.

Solving similarly for the penumbra,

$$L_p/R_e = (L_{se} - L_p)/R_{sun}. \quad (4)$$

This reduces to

$$L_p = L_{se}/(R_{sun}/R_e + 1) \quad (5)$$

And evaluates to

$$L_p = 1,360,000. \quad (6)$$

Note that the "apex" of the penumbra is between earth and sun but that the effect of the penumbra (partial obscuration) only occurs behind the earth. Penumbral calculations are only included here so that the degree of error introduced by ignoring partial eclipsing can be determined.

Both cones may be described by the revolution of triangles which have an acute angle at the apex of the cone and at the center of the earth and a right angle at the surface of the earth. Refer to the angle at the center of the earth between the shadow center line and the line touching the edge of the umbra at satellite altitude as A_u . See Figure 6. For the penumbra, the equivalent angle is A_p . When the satellite position vector to shadow centerline angle is greater than A_p , the satellite is fully illuminated. When the satellite is between A_p and A_u , it is partially illuminated. When it is less than A_u , the satellite is fully eclipsed.

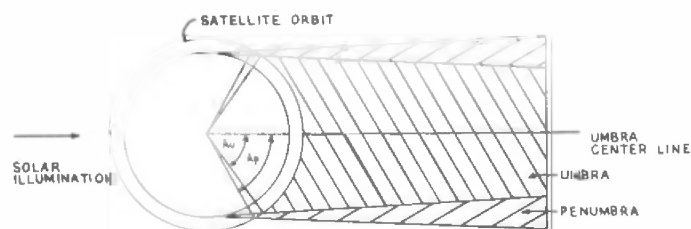


Figure 6. Eclipse Model
Not to Scale

Solving the triangle with knowledge of which angles are obtuse and acute by the definition of the problem, the following formulae for these angles, measured from the centerline are derived.

$$A_u = \arcsin(R_e/R_s) - \arcsin(R_e/L_u) \quad (7)$$

and

$$A_p = \arcsin(R_e/L_p) - \arcsin(R_e/R_s) \quad (8)$$

where R_s is the distance of the satellite from the center of the earth.

These evaluate to the angles in degrees given in Table 11. Other parameters and cases for various interesting orbits are given. Time spent in partial illumination amounts to seconds per orbit at low altitudes. Therefore, only the umbra or eclipsing totality is considered in the remainder of this analysis.

The "footprint" of the satellite is described by the "radius" of the ground coverage that it enjoys from its altitude. This "radius" is given in degrees of latitude.

The "worst case eclipse time" assumes a circular orbit of altitude and period given and that the satellite passes directly through the center of the umbra, remaining in the dark as long as possible.

The "best pass" occurs only when the satellite passes directly overhead from the observer.

For any orbit that is not sun synchronous, worst case eclipsing will occur at some inevitable combination of season and orbital configuration. This is because the ascending node precesses with respect to the sun and the satellite path will precess through the umbra center line periodically.

Table 11—Parameters of Interest for Various Orbits

Altitude Case	A_u rad/ deg	A_p	Period min	Footprint rad/deg	Eclipse worst min	Pass best min
Earth's surface	89.7	90.2	84.5	0.0	42.1	0.0
300 Km (PTSE deploy)	72.5	73.0	90.5	17.2	36.5	8.7
800 Km (OSCAR 8 type)	62.4	63.0	100.9	27.3	35.0	15.3
8950 Km (PTSE Phase 2)	24.3	24.9	314.8	65.4	42.5*	114.4
Geosynchronous	8.4	9.0	1440.0	81.3	67.2*	—
Moon distance	0.6	1.2	41961.3	89.1	139.9*	—

(* Partial eclipsing is significant in these cases.)

The position of the sun, as seen from an inertial earth, changes by 0.9856 degrees per day in the same direction as earth rotation. This makes the solar day slightly longer than the inertial or sidereal day. Because the earth is not a perfect sphere but is slightly flattened at the poles, the ascending node of orbiting satellites is observed to precess in inertial space. For prograde orbits, those with inclinations between 0 and 90 degrees, this precession is in the opposite direction from the apparent change of the sun's location. For retrograde orbits, those with

inclinations between 90 and 180 degrees, this precession is in the same direction with the sun's apparent change of location and can be fine tuned to cancel it out for all practical purposes. This means that the satellite orbit stays fixed over a particular solar local time.

The amount of precession is a function of altitude, eccentricity, and inclination. For circular orbits at altitudes below 6000 Km, inclinations are possible which are sun synchronous.

Table 12—Sun Synchronous Circular Orbit Inclinations

Altitude	Inclination
300 Km	96.7
800 Km	98.6
> 6000 Km	not possible

A sun synchronous orbit near the terminator (as were the orbits of Oscars 6, 7, and 8) contains little eclipsing during some seasons and no eclipsing at others. It is also convenient for amateur radio operator scheduling, in that passes occur over the mid morning and early evening hours daily. It is unlikely that PTSE-H will be given, or will be able to achieve, a sun synchronous orbit. It is also cited below that such an orbit does not even nearly

maximize coverage for users at moderate latitudes.

Table 13—Effect of Precession of the Ascending Node for Orbit Inclination of 57 Degrees

Altitude Km	Drift deg/day	Local Time Below Node Change in minutes/day	Half Cycle days
300	-5.60	-22.4	16
800	-4.57	-18.3	20
8950	-1.24	-4.95	73

The "half cycle" is how often the orbit precesses through the umbra center line or through some other solar referenced position. See Figure 7.

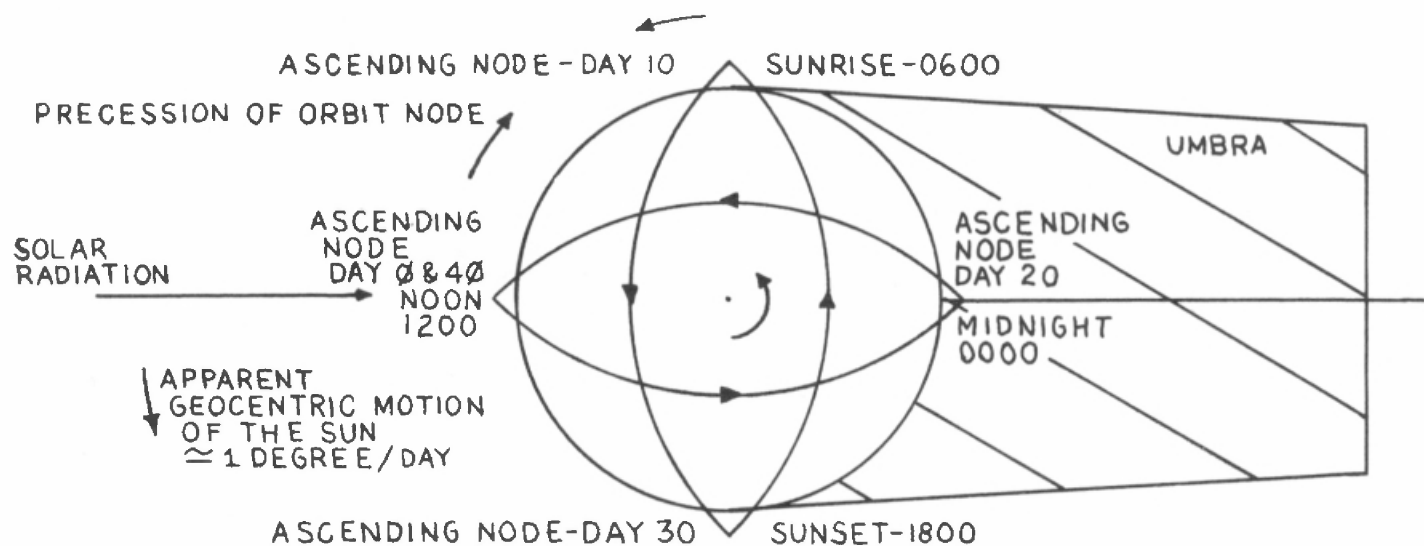


Figure 7. Precession of Ascending Node
View from over North Pole
Not to Scale
Times are Local Solar

Since the umbra center line moves between latitudes 23.5 south and 23.5 north, a range which includes the equator, and since all orbits must cross or lie on the equator, this precession forces all orbits (that are not sun synchronous) to experience periods of worst case eclipsing.

Minimal eclipsing depends on inclination. When the latitude of the umbra centerline is near a maximum, such as 23.5 degrees south at the beginning of summer in the

northern hemisphere, nodal precession will take the highest satellite latitude to a point over local midnight. In the case of a 57 degree inclination, this means that the subsatellite point never gets closer than $23.5 + 57 = 80.5$ degrees of latitude from the shadow centerline. Since this is greater than the 62.4 degree umbra radius at 800 Km altitude, no eclipsing will occur. Eclipsing times for intermediate cases are developed in the following formulations.

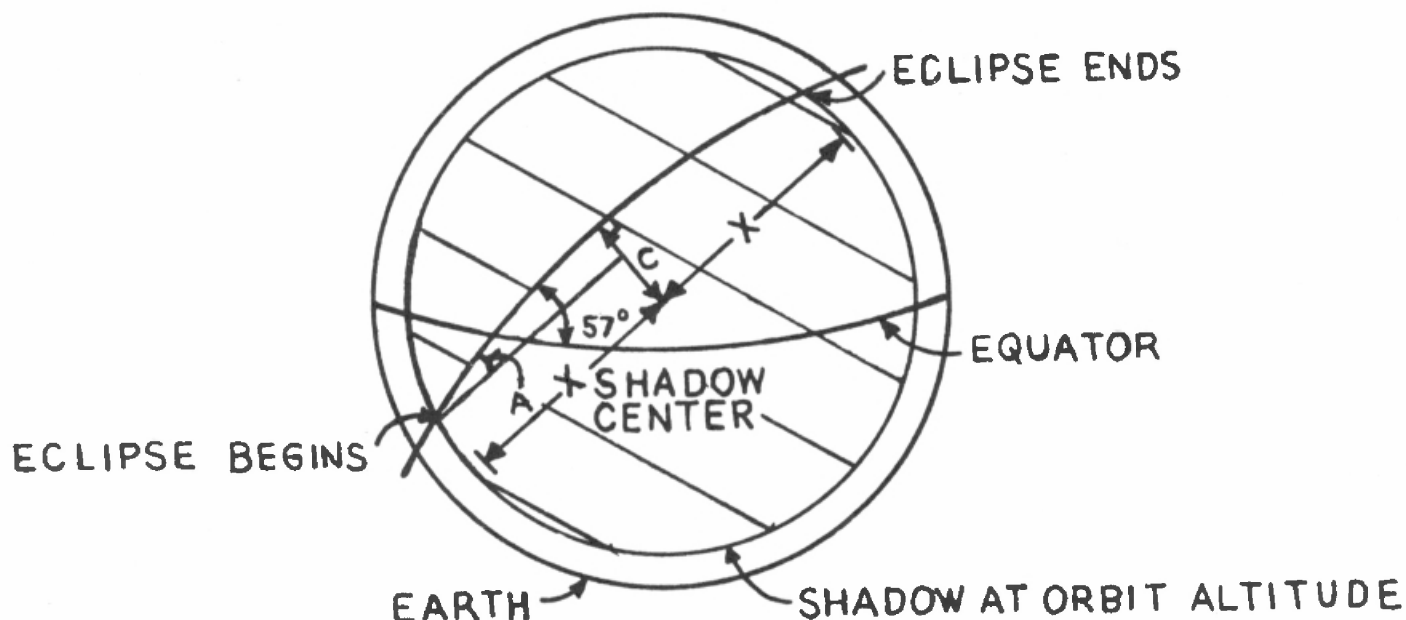


Figure 8. Geometry of Passage Through Shadow

c = Closest Approach to Shadow Centerline, Arc

$2x$ = Amount of Orbit Spent in Shadow, Arc

See Equations 9-14

Refer to Figure 8. From spherical trigonometry, the amount of specific anomaly spent in eclipse is $2x$ where

$$x = \arcsin (\tan(c) / \tan(A)) \quad (9)$$

and

$$A = \arcsin (\sin(c)/\sin(Au)). \quad (10)$$

The angle between the umbra centerline and the satellite path's closest approach to centerline is " c ." All angles are in the first quadrant. Worst case eclipsing occurs at $c = 0$. For this case, the first equation is undefined (because $A = c = 0$) and

$$x = Au. \quad (11)$$

If a case occurs where $c > Au$, the second equation is undefined and

$$x = 0. \quad (12)$$

Time spent in eclipse per circular orbit is

$$x * \text{period} / 180 \text{ degrees}. \quad (13)$$

The fraction of mean anomaly (or time for a circular orbit) spent in eclipsing is

$$x / 180 \text{ degrees}. \quad (14)$$

Now, total power available may be computed for best and worst case eclipsing for both stabilization cases, and typical scenarios may be discussed.

For the 800 Km, 57 degree inclination orbit, the best case given above will occur near the beginning of summer and winter when the earth's shadow is centered at highest latitude. For many months of the year, the shadow is centered at latitudes nearer to or on the

equator. At these times there is always some eclipsing. When the earth's shadow is centered over the equator at the beginning of spring and fall, the satellite closest approach to the shadow center cannot be greater than the inclination of 57 degrees. For this condition, $x = 31.7$ degrees from the above equations. This corresponds to 17.6% eclipsing or 17.8 minutes per orbit in darkness and is the minimum possible at that time of year.

Now consider the two stabilization cases, inertial and geocentric. If power collection is to be emphasized, the spacecraft will be inertially stabilized and maintained broad side to solar energy. Assume that the rotation axis can always be held within 30 degrees of normal to solar radiation. For this case

$$(29.0 \text{ watts incident} * \cos (30)) = 25.1 \text{ watts}$$

This is the minimum amount that will be collected whenever the satellite is illuminated.

If directional antenna coverage is to be emphasized, gravity gradient or some other geocentric stabilization may be employed so as to fix a facet of the satellite with respect to the earth. Presumably, the satellite longitudinal axis would be aimed toward the center of the earth at all times. Whether the satellite could also spin on the longitudinal axis while maintaining this geocentric attitude is beyond the scope of this study but is certainly a thermal concern.

When the spacecraft orbit is near the terminator, the solar collection angle will tend to be as good for this case as it is for the solar energy collection emphasis case given above. For instance, in the best case given above, where the satellite never passes closer than 80.5 degrees from earth shadow center line, the angle of incidence

of solar radiation will vary from 0 degrees (from normal) over the equator to 9.5 degrees (from normal) at the extreme latitudes. Additionally, there is no eclipsing in this situation.

When the spacecraft orbit is at worst case eclipsing, this stabilization mode exacerbates the power shortage problem. When the spacecraft is over the terminator, shortly after its sunrise or before its sunset, solar incidence is again 0 degrees from normal, but as it passes over the subsolar point, the top of the satellite is illuminated, no solar radiation is seen by the cells on the sides at all. The average power available under this worst case situation is

$$(29.0 \text{ watts incident} / \pi) * \int_{m=90}^{m=0} (\cos(m)) dm \quad (15)$$

$$m = Au - 90$$

where Au was determined in equation (7) above. See Figure 9.

This evaluates to

$$(29.0 \text{ watts incident} * (1 + \cos(Au)) / 3.14 = 13.5 \text{ watts}$$

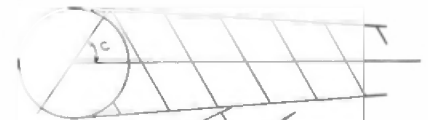
taken over the entire orbit including the worst case eclipse itself.

The general solution for average power where the minimum angle at earth center of the orbit path from shadow centerline, "c," is known as

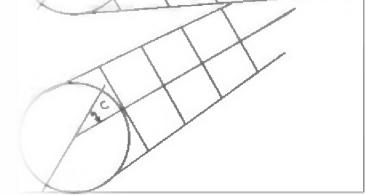
$$(29.0 \text{ watts} / \pi) * \int_{m=x-90}^{m=90} \cos(\arcsin(\sin(m) * \cos(c))) dm \quad (16)$$

$$m = x - 90$$

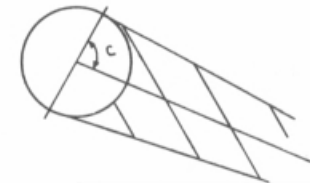
A) EQUINOX BEST CASE
C = 57° = INCLINATION
ECLIPSE = 17.6 %



B) SOLSTICE
'POOR' BEST CASE
C = 33.5°
ECLIPSE = 31.3 %



C) SOLSTICE
BEST BEST CASE
C = 80.5°
ECLIPSE = 0 %



D) WORST CASE
OCCURS YEAR AROUND
EVERY 20 DAYS
C = 0°
ECLIPSE = 34.7 %

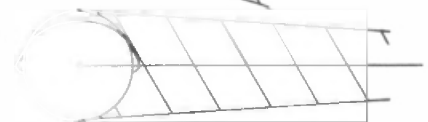


Figure 10. Eclipsing Cases
See Tables 14, 15 and 16

where "x" is determined in equations 9, 11, and 12 above. Note that for $c = 90$ degrees, this reduces to equation (15).

The effects of eclipsing and orientation can now be summarized. See Figure 10.

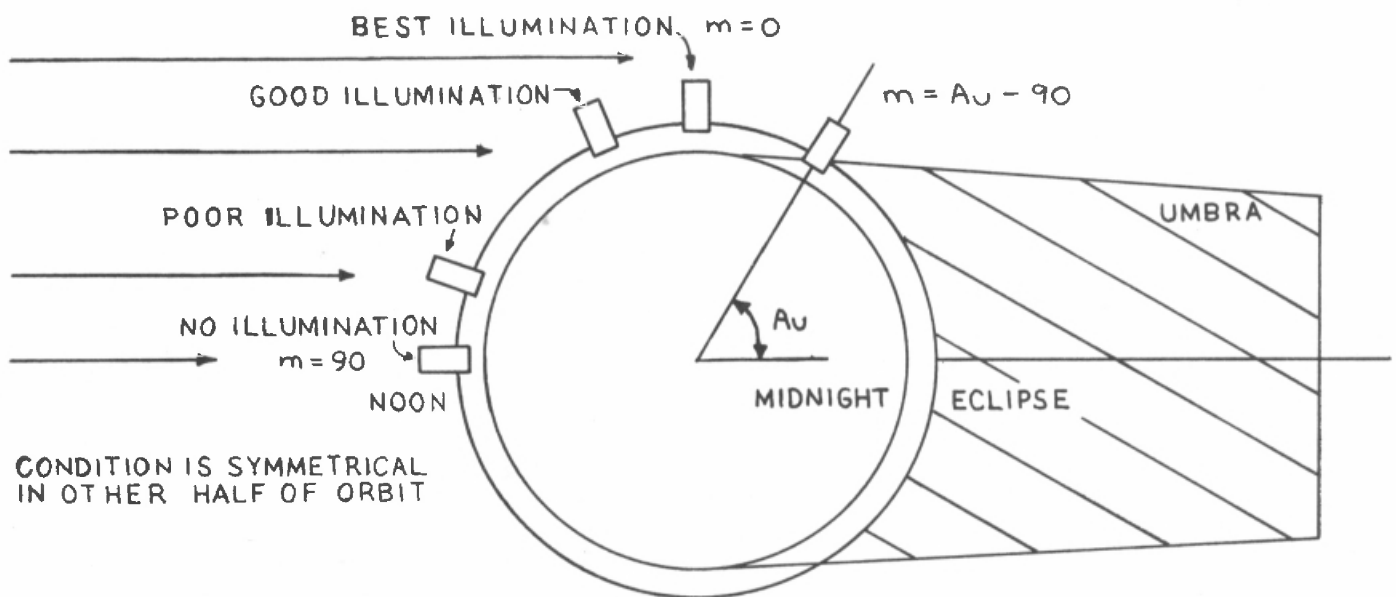


Figure 9. Worst Case Exposure in Geocentric Attitude
See Equations 15 and 16

Table 14—Best and Worst Case Average Power Available

Season	Case	Eclipse	Average Power, Watts		
			inertial	geocentric	possible
Equinox	Best	17.6%	20.7	22.4	23.9
Solstice	Best	none	25.1	28.8	29.0
Any	Worst	34.7%	16.4	13.5	18.9

The “inertial” cases include the 30 degrees off-normal attitude adjustment. The “possible” cases do not include this adjustment.

Now, using the precession figures given in Table 13, typical seasonal situations can be approximated. The ascending node precesses 90 degrees relative to the sun about every 10 days (half of a “half-cycle”). In Tables 15 and 16, the effects of nodal precession on the power availability situation are seen for different times of year. The local time below ascending node simply indicates the orientation of the orbit with respect to the sun.

For 0000 or 1200 (midnight or noon), the orbit passes through or very near the earth shadow centerline. This results in maximum eclipsing and worst case power collection for geocentric stabilization. For 0600 or 1800 (terminator, sunrise or sunset), the orbit passes through the earth shadow at high latitudes. In alternate occurrences, shadow center latitude and satellite latitude are in opposite hemispheres and minimum eclipsing for that time of year occurs.

To compute values of “c” for the tables, there are three cases.

For ascending node over 0600 local sunrise, the satellite crosses midnight at its southernmost point. Thus, if sun declination is positive, shadow centerline is south and the declination (absolute value) is subtracted

from inclination. If sun declination is negative, add the declination (absolute value) to inclination.

For ascending node over 1800 local, sunset, the opposite is true. For these two cases, see Figure 10.

For ascending node over local noon or midnight, shadow center will be on the longitude of midnight but not necessarily on the equator where the satellite path crosses. See Figure 11. Construct a triangle with the line from equator crossing to shadow center as the hypotenuse. The length (in arc) of this side is the sun declination. The included angle at the node is $90 - \text{inclination}$, or 33 degrees in the case of 57 degrees inclination. The right angle is at the satellite position of closest approach to the shadow center. By the law of sines for spherical trigonometry,

$$c = \arcsin(\sin(\text{declination}) * \sin(33 \text{ degrees}))$$

Signs are not important in this calculation since “c” is an absolute quantity and is always positive or zero.

The orbit actually passes through the shadow center line a few days or hours earlier or later resulting in worst case eclipsing for every cycle.

Sun declinations are obtained from the 1987 World Almanac.

Roughly speaking, near equinox a cycle of about 10 days of poor illumination is followed by about 10 days of fair to good illumination. Near solstice a cycle of about 10 days of good illumination is followed by about 30 days of poor illumination.

Geocentric stabilization allows slightly less power than best case inertial stabilization under good conditions and is somewhat worse at times of worst case eclipsing. A 30 degree aiming error in inertial stabilization makes the two cases similar but geocentric stabilization exaggerates the extremes.

These charts represent the local peaks and valleys in the cycles. A graph of the eclipsing and power gathering situation would connect the points with smooth curves.

This analysis does not answer all possible questions concerning the satellite power budget, but it is clear that worst case eclipsing should be expected on a regular and sometimes prolonged basis. The satellite operating schedule may need to be varied from week to week to accommodate the ever changing power collection situation.

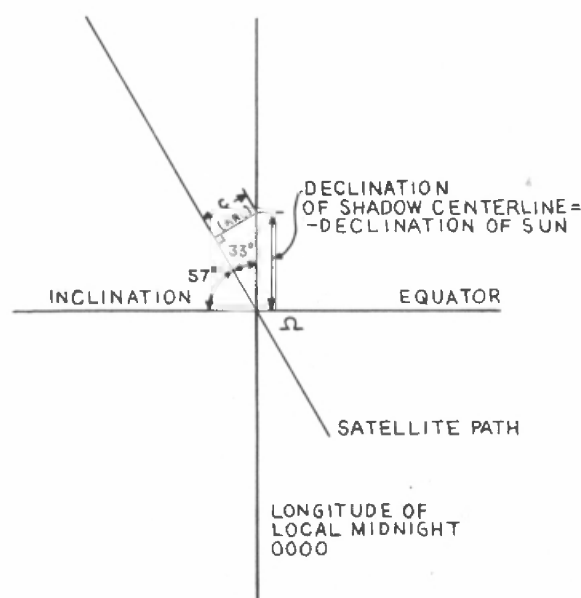


Figure 11. Computing C When Ascending or Descending Node is Over Local Midnight

Table 15—Power Available Near Equinox

Date	Local Time at asc. node	Sun decl	c deg	Eclipsing percent	Power, Watts	
					inertial	geocentric
19 Feb	1200	-11.6	6.3	34.6	16.4	13.8
01 Mar	0600	- 7.9	64.9	0.0	25.1	27.6
11 Mar	0000	- 4.0	2.2	34.7	16.4	13.6
21 Mar	1800	0.1	57.1	17.5	20.7	22.5
31 Mar	1200	+ 3.9	2.1	34.7	16.4	13.6
10 Apr	0600	+ 7.7	49.3	24.9	18.9	19.9
20 Apr	0000	+11.3	6.1	34.6	16.4	13.8
30 Apr	1800	+14.6	71.6	0.0	25.1	28.3

A similar situation occurs in August, September and October.

Table 16—Power Available Near Solstice

Date	Local Time at asc. node	Sun decl	c deg	Eclipsing percent	Power, Watts	
					inertial	geocentric
22 May	1200	+ 20.2	10.8	34.4	16.5	14.1
01 Jun	0600	+ 22.0	35.9	30.6	17.4	17.1
11 Jun	0000	+ 23.0	12.3	34.3	16.5	14.2
21 Jun	1800	+ 23.4	80.4	0.0	25.1	28.8
01 Jul	1200	+ 23.2	12.4	34.3	16.5	14.2
11 Jul	0600	+ 22.2	34.8	30.9	17.4	17.0
21 Jul	0000	+ 20.6	11.0	34.4	16.5	14.1
31 Jul	1800	+ 18.5	75.5	0.0	25.1	28.5

A similar situation occurs in November, December, and January.

Comparison of Power Required to Power Available

Table 10 is duplicated here for ease of reference.

Table 10—Power Requirements Summary

Operating Mode	Power, Watts	Energy/Day, KJoules
full user access	25.0	2160
recharge	5.9	510
maneuvers	10.0	864

From the figures given, it is clear that the mission objective of full user access and full memory utilization can only be achieved by careful and probably clever control of the power system and scheduling of spacecraft system sleep or off modes.

For normal user access periods, the power budget is

tight for the best case and negative in all others for the library computer duty cycle used in the estimates. Mission planning and hardware design must emphasize the ability to conserve significantly at this point.

As long as the satellite is stabilized properly, there is always at least a 7.6 watt margin in recharge mode. This means that, if all else fails, the mission can be continued by limiting user access while all library memory remains powered.

During maneuvers, the satellite will probably be inertially stabilized in an orientation required by the maneuvers. If the angle of incidence of solar radiation goes above about 60 degrees in such an orientation, power available may not meet power required. Fortunately, cases where maneuvering orientation may be outside this limit are not cases where worst case eclipsing will occur. On the other hand, some maneuvering may occur at lower orbital altitudes where eclipsing is more severe.

Conclusions

The efficiency model of the solar cell/battery system has only been mentioned here and has not been incorporated into the figures. As this model is developed, the power available figures are likely to go down.

It is understood that a satellite operates on collected or stored energy of which power is a continuous time manifestation. In later analyses, it may be more meaningful to talk of Joules collected per day or amp-hours at some stated bus voltage. To find energy amounts per day from the average power figures given, multiply watts by 86,400 seconds per day. To find amp-hours, divide by 24 hours per day then divide by bus voltage.

Power system degradation has also been mentioned but not included. Because the power budget is so tight, as soon as solar cell and battery performance begin to deteriorate, the effects will be felt acutely. At some point in the mission, it may be necessary to go to energy collection emphasis orientation and stabilization at the expense of antenna coverage. RF and antenna systems should be designed with this in mind. Solar cells could be placed on "top" (away from the earth) to help with available power if geocentric stabilization is used and if a rocket nozzle is not present on this facet. If it com-

pletely covered the top facet, such an array might provide up to 16.7 watts when the satellite was fully illuminated directly from the top. The cells would not be illuminated when the longitudinal axis was normal to incident energy.

The results of this study can and should be refined by expanding the scope and accuracy of the various analyses. There are at least three areas in which refinements are needed:

- 1) the battery - solar cell model,
- 2) spacecraft maneuvering equipment, and
- 3) user demographics.

In this last area, a computer model of the satellite orbit combined with a database of user populations and locations around the world would give the capability to model the mission weeks or months at a time yielding library storage requirements, power acquired, and power consumed, both as averages and as absolute peaks and valleys. This would give a feel for required energy storage depth and severity of overcharge. An adequate user database would consist only of expected packet radio populations associated with a central location per country, state, or province and expected traffic levels within and between the areas. Refinements could include the "prime time effect."

A Non-Cosmetic Improvement to the W3IWI Tracking Algorithm

Part I: Theoretical development of a fast finder of AOS times

by

Robert W. McGwier, N4HY

Abstract

Theoretical development is given for an algorithm for a major improvement in search times for acquisition of signal times when given the Keplerian elements of a satellite, and the latitude, longitude and height above sea level of a ground station. Elementary differential calculus and analytic geometry together with a Keplerian description of orbital dynamics are combined to derive a closed-form solution to the problem of finding AOS and LOS times in eccentric anomaly rather than directly in time. This relieves us of the expense of solving Kepler's equation at each step in finding these times of interest. Part II will describe our work on the implementation of this algorithm.

Introduction

Since *Orbit* No. 6 [1], we have had many versions of Tom Clark's effort in computer tracking for amateur satellites (the now-famous W3IWI program). The home computer has become an integral part of the amateur satellite user's equipment and one of the current trends in the home computer (and all other parts of the computer industry for that matter) is to larger machines in terms of addressable memory. This extra memory allows us for the first time to add many additions to the IWI program that are not just cosmetic. Most would agree that up until recently, the only changes have been cosmetic. The worst feature of this program is the amount of time it spends in a linear search for the next acquisition of signal from the time input to the step-search algorithm. We will describe here recent efforts to use the elementary differential calculus and some analytic geometry to greatly improve the speed of finding the "next pass."

We will present a Keplerian closed-form solution originally derived by Pedro Escobal [2], and adapted by us into a general purpose tracking algorithm: Quiktrak[™] [3]. In the past, it has been the custom to find the next acquisition of signal (hereafter known as AOS or "pass") by letting the computer run through its ephemeris for a given satellite at a fixed time step, checking at each step whether or not the satellite elevation was greater than some minimum value. By attacking the problem from a slightly different point of view, that of letting Eccentric Anomaly be the independent variable, it is possible to arrive at a closed form solution to the satellite visibility problem. We get a transcendental equation (like Kepler's equation) in the eccentric anomaly corresponding to AOS or loss of sig-

nal (hereafter LOS). We will find it more difficult to solve than Kepler's equation and thus algorithmically a great deal more complex to solve. *However*, we only have to solve it once (!) for each AOS. If we are on the westernmost pass of a low earth polar orbiting satellite from mid-latitudes, and we have our time step set at a few minutes for the older step search method, we may have to solve Kepler's equation around a hundred times depending on the semi-major axis and the exact time step.

Theoretical Development

Suppose we let ρ be the vector connecting the ground station to the satellite of interest. The sin of the elevation h is given by

$$(1) \quad \frac{\rho}{|\rho|} \cdot Z = \sin(h)$$

where Z is that vector which points at the zenith at the station location (geodetic zenith on the adopted ellipsoid for the earth at the station's latitude and longitude). We will refer Z to an inertial reference frame, the right ascension-declination coordinate system (hereafter known as RAD) which is that coordinate system that referred to the "fixed stars." Let θ_0 be the sidereal time of the ground station at some fixed epoch. Let ϕ be the ground station geodetic latitude, λ_E the station East longitude, and H be the station height above the figure adopted for the earth. (For our purposes the height above sea level is adequate.) We may proceed to derive the rise-set equation for the satellite. Let Z be resolved in the RAD.

The coordinates are given by

$$(2) \quad \begin{aligned} Z_x &= \cos(\theta)\cos(\phi) \\ Z_y &= \sin(\theta)\cos(\phi) \\ Z_z &= \sin(\phi). \end{aligned}$$

Here θ is the station sidereal time, and ϕ is the geodetic latitude of the ground station. Let

ρ = slant range vector

R = station coordinate vector

and,

r = orbit radius vector.

The slant range vector is that vector pointing from the

ground station to the satellite with length equal to the slant range. The station coordinate is that vector which points from the ground station to the center of the earth. The orbit radius points from the center of the earth to the satellite. From this we see that

$$(3) \quad \rho = \mathbf{r} + \mathbf{R}.$$

In terms of the geodetic latitude, components of the $\mathbf{R}$ vector

$$X = -G_1 \cos(\phi) \cos(\theta)$$

$$Y = -G_1 \cos(\phi) \sin(\theta)$$

$$Z = -G_2 \sin(\phi)$$

where

$$G_1 \equiv \frac{a_e}{\sqrt{1 - (2f - f^2) \sin^2(\phi)}} + H$$

$$G_2 \equiv \frac{(1 - f)^2 a_e}{\sqrt{1 - (2f - f^2) \sin^2(\phi)}} + H$$

and a_e is the equatorial radius of the earth, f is the flattening of the ellipsoid adopted for the earth, H is station elevation above sea level (the adopted ellipsoid), and θ is the station local sidereal time. Having set up the necessary variables in the proper coordinate systems we may rewrite equation (3) in component form and then substitute into equation (1). From this process we get

$$(4) \quad (x+X)Z_x + (y+Y)Z_y + (z+Z)Z_z = \rho \sin(h).$$

If we let Z be the unit vector pointing to the zenith as described earlier and X, Y, Z be the station coordinates as above we get

$$(5) \quad \begin{aligned} & [x - G_1 \cos(\phi) \cos(\theta)] \cos(\phi) \cos(\theta) + \\ & [y - G_1 \cos(\phi) \sin(\theta)] \cos(\phi) \sin(\theta) + \\ & [z - G_2 \sin(\phi)] \sin(\phi) = \rho \sin(h). \end{aligned}$$

Upon rearrangement we arrive at

$$(6) \quad \begin{aligned} & x \cos(\phi) \cos(\theta) + y \cos(\phi) \sin(\theta) + z \sin(\phi) \\ & = \rho \sin(h) + G \end{aligned}$$

where

$$G = G_1 \cos^2(\phi) + G_2 \sin^2(\phi).$$

This process looks fairly complicated but in actuality is picking out one of the simplest objects in geometry. This is the equation for a cone. A very particular cone however. This cone has its apex on the earth at the location of the ground station and the central axis of this right circular cone is the vector pointing to the zenith at the location of the ground station. This cone stays fixed in the local rotating coordinate system. If a vector (x, y, z) lies inside this cone it is above the station's

horizon. When it is outside the cone it is below the horizon. Our task is to find those x, y , and z for our satellites which lie exactly on the cone because this will define an AOS or an LOS. By complicating our expression only slightly with the presence of $h=0$, and the use of a right circular cone instead of a plane, we have allowed for the fact that the ground station might be in a depression and his actual horizon is above the ideal horizon by an angle h .

Let us use the standard Keplerian elements to describe the geometry of the orbit of our satellite. Let ω be the argument of perigee, Ω is the right ascension of the ascending node, i the inclination. From these numbers we may derive useful vectors describing the plane of the orbit of the satellite about the earth. Let $\mathbf{P}$ be the vector given by

$$(6) \quad \begin{aligned} P_x &= \cos(\omega) \cos(\Omega) - \sin(\omega) \sin(\Omega) \cos(i) \\ P_y &= \cos(\omega) \cos(\Omega) + \sin(\omega) \cos(\Omega) \cos(i) \\ P_z &= \sin(\omega) \sin(i). \end{aligned}$$

Let $\mathbf{Q}$ be the vector given by

$$(7) \quad \begin{aligned} Q_x &= -\sin(\omega) \cos(\Omega) - \cos(\omega) \sin(\Omega) \cos(i) \\ Q_y &= -\sin(\omega) \cos(\Omega) + \cos(\omega) \cos(\Omega) \cos(i) \\ Q_z &= \cos(\omega) \sin(i). \end{aligned}$$

For those of you who do not recognize these quantities, these are the columns of the matrix $\mathbf{C}$ as defined by Clark in his tracking algorithm. There is another vector usually called $\mathbf{W}$ in this triad which we do not need and will not define. One could easily follow the development of the next few quantities in Clark's algorithm but we include them for our final development. Let

$$x_\omega = a(\cos(E) - e)$$

$$y_\omega = a\sqrt{1 - e^2} \sin(E).$$

Where a is the semimajor axis of the orbit of our satellite, E is the eccentric anomaly, and e is the eccentricity. For the remainder of the argument we will simplify our expression by taking the angle of the ground station horizon with respect to the plane tangent on the ellipsoid representing the earth's surface to be zero. In other words we assume that the ground station is an ideal location with no hills, etc. This is the ground station type which is in the final program. Our "cone" has degenerated to a plane. The plane is defined by the vector normal to it, the vector pointing to the ground station's zenith. Upon substitution of our formulas for $\mathbf{r}$ in terms of $x_\omega, y_\omega, \mathbf{P}$, and $\mathbf{Q}$ into our equation (6), which has been transformed into the " ω " coordinate system we get

$$(7) \quad \mathbf{P} \cdot \mathbf{Z} x_\omega + \mathbf{Q} \cdot \mathbf{Z} y_\omega = G.$$

Here

$$\mathbf{P} \cdot \mathbf{Z} = P_x \cos(\phi) \cos(\theta) + P_y \cos(\phi) \sin(\theta) + P_z \sin(\phi)$$

and likewise for $\mathbf{Q} \cdot \mathbf{Z}$. Substituting the formulas for x_ω and y_ω into the left hand side of (7) and subtracting the right hand side gives us the function we are interested in

$$F \equiv a(\cos(E) - e)\mathbf{P} \cdot \mathbf{Z} + (a\sqrt{1 - e^2}\sin(E))\mathbf{Q} \cdot \mathbf{Z} - G.$$

When this function is zero we have a bird on the horizon of the ground station. $\mathbf{P} \cdot \mathbf{Z}$ and $\mathbf{Q} \cdot \mathbf{Z}$ are time-dependent and we must rewrite these in terms of the eccentric anomaly. Given local sidereal time is θ_0 at universal time t_0 we get

$$Z_x = \cos(\phi)\cos\left[\theta_0 + \frac{d\theta}{dt}(t - t_0)\right]$$

$$Z_y = \cos(\phi)\sin\left[\theta_0 + \frac{d\theta}{dt}(t - t_0)\right]$$

$$Z_z = \sin(\phi)$$

where

$$\frac{d\theta}{dt} = \text{ratio of length of sidereal second to universal second}$$

and

$$t = \text{universal time.}$$

Introducing the relationship between time and dynamics (Kepler's equation) we find

$$(8) \quad t = \frac{E - e \sin(E)}{n} + T$$

where

$$n = \text{mean motion}$$

and

$$T = \text{time of latest perigee passage.}$$

This gives us a new representation of the $\mathbf{Z}$ vector in terms of E .

$$Z_x = \cos(\phi)\cos\left(\theta_0 + \frac{d\theta}{dt}\left[\frac{E - e \sin(E)}{n} + T - t_0\right]\right)$$

$$Z_y = \cos(\phi)\sin\left(\theta_0 + \frac{d\theta}{dt}\left[\frac{E - e \sin(E)}{n} + T - t_0\right]\right)$$

and Z_z is as before. Time has been eliminated and the new independent variable is eccentric anomaly. A solution to $F(E) = 0$ will be either an AOS or an LOS. If the derivative of F is positive at the crossing of the zero line then, this is an AOS and the opposite for LOS. Given some initial guess E_1 for the eccentric anomaly of an AOS, we may use Newton's method to find the eccentric anomaly of a zero crossing (and thus an AOS or LOS) using the formula

$$E_{n+1} = E_n - \frac{F(E)}{F'(E)} \quad n = 1, 2, 3, 4, 5, \dots$$

Where

$$\begin{aligned} F'(E) = & \left[a(\cos(E) - e)(P_y Z_x - P_x Z_y) \right. \\ & \left. + a\sqrt{1 - e^2} \sin(E)(Q_y Z_x - Q_x Z_y) \right] \\ (9) \quad & \times \frac{(1 - e \cos(E))}{n} \theta + \mathbf{Q} \cdot \mathbf{Z} a\sqrt{1 - e^2} \cos(E) \\ & - \mathbf{P} \cdot \mathbf{Z} a \sin(E). \end{aligned}$$

The implementation of this algorithm must take into account the differing behavior of the function $F(E)$ for different types of orbits. In the end, this worked out to about five different classes of orbits and/or situations. The descriptions of the implementation will be left for part II.

The amateur satellite community owes Tom Clark a large vote of thanks for his original work on the IWI tracking algorithm. I might add that had he not put the program in the conceptual framework that he did, the adaptation of the early work of Escobal to this program would have been a great deal more difficult.

Bibliography

- [1] Tom Clark, "Basic Orbits," *Orbit*, No. 6, page 6.
- [2] Pedro Escobal, "Rise and Set Time About an Oblate Planet," *AIAA Journal*, Vol. 1, No. 10, October 1963.
- [3] Quiktrak[™] is available from the AMSAT Software Exchange for a growing number of computers. AMSAT S.E., P.O. Box 27, Washington, D.C. 20077 and SASE.